MICRO AND TELEVISION PROJECTS

BY TREVOR BROWN

BRITISH AMATEUR TELEVISION CLUB

ACKNOWLEDGEMENTS

The Engineers

Trevor Brown G8CJS
Clifford Brownbridge G6BIN
Richard Russell G4BAU
Jacques Pochet F6BQP
John Lawrence GW3JGA
David E Jones GW8PBX

The Draughtsmen

John Wood G3YQC
Tony Marsden G6JAT

The Writers

Andrew Emmerson G8PTH
Dave Halliday
Peter Delaney G8KZG
Peter Ward G4GYI

Prototypes

Chris Lewis G6ACL

Software

Robin Stephens G8XEU

CONTENTS

PREFACE

This publication covers a very wide range of Television Projects and pays particular attention to the role the home computer can play in Television. The projects range from the simple to the advanced, with a range of printed circuit boards being made available to ease any constructional difficulties. All the software featured has been specially written and lots more is in the pipeline and will be made available via CQ-TV the B.A.T.C.'s quarterly publication.

Teletron is an attempt at launching a very flexible micro controller card for use in Television applications. It is hoped to support this card with plug in software and plug in modules, the accompaning VDU is designed to work with a feed of mixed sync for locking purposes and will not function without.

This publication also incorporates the popular Electronic Test Card and PAL coder from the original and no longer produced Amateur Television Handbook. A Secam Coder designed by Jacques Pochet has also been introduced for which a plug in Printed Circuit Card is available from him, this module is pin compatible with the PAL Coder and enables Secam operation by a simple module change.

Time scale is always a problem when putting together a publication like this and one problem which has developed is a Texas chip the 74S262 which was new at the outset and seems to be becomming scarce, should this problem not resolve itself then alternative Engineering will be introduced. Please contact Members Services for any such supply problems.

I hope you will all find Micro and Television Projects an interesting and stimulating publication.

TREVOR BROWN

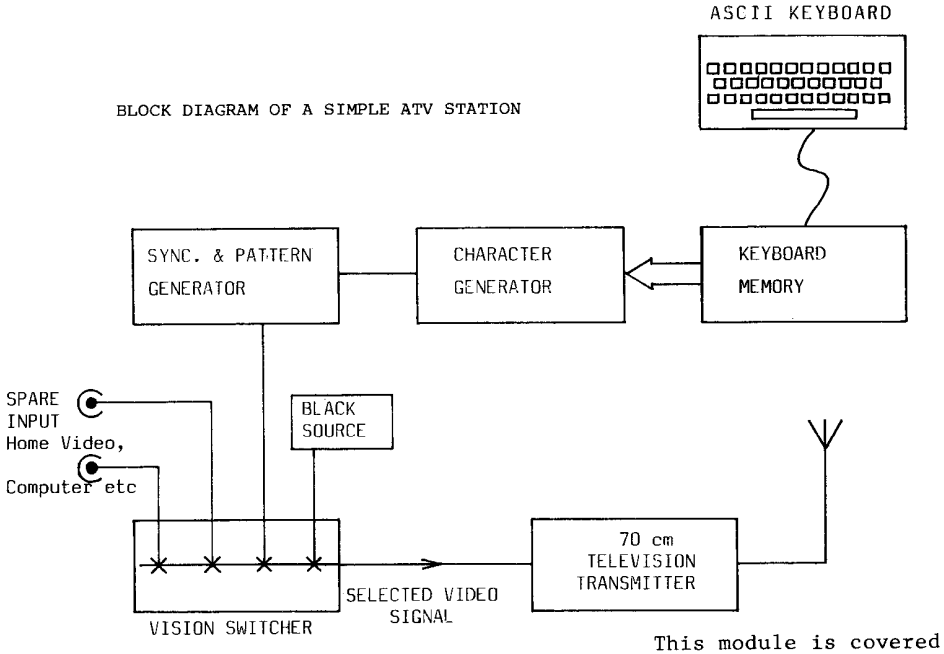
PCB PROJECT

CHAPTER 1
A SIMPLE ATV STATION
TEST PATTERN & SYNC GENERATOR

This is the first module in our simple TV station and is the 'heart' of the system, providing the master timing signals to which the rest of the picture sources are synchronised. It also provides the TV test waveforms which are essential for checking out and setting up the rest of the station.

Of these waveforms the most useful is the grey scale or 'staircase' signal, which is used to measure the linearity of video processing circuits. The crosshatch or grille is also useful, particularly for checking the geometry of your TV monitor and receiver.

BLOCK DIAGRAM OF A SIMPLE ATV STATION



This module is covered in TV for Amateurs

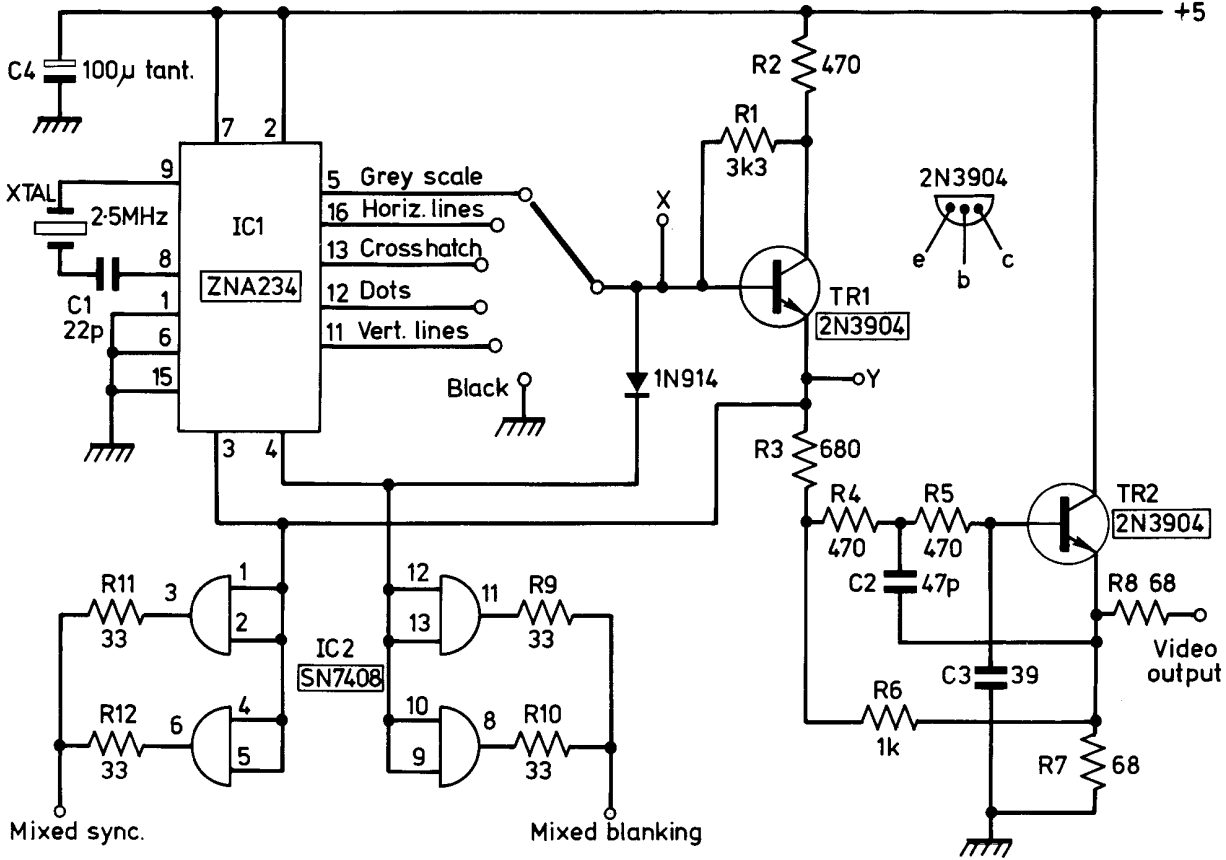


FIG. 1. 625 line t.v. pattern and sync generator.

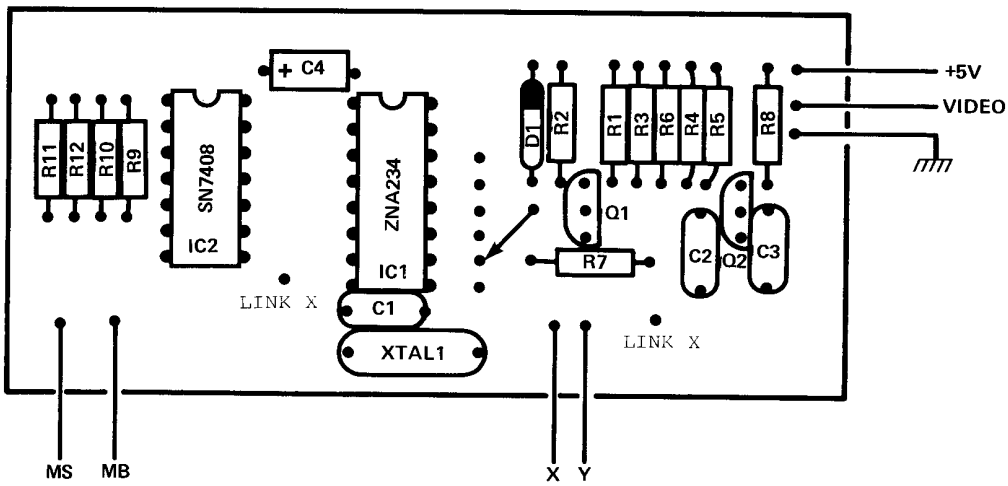
The circuit revolves around the Ferranti Pattern Generator IC, ZNA 234. All the waveforms required are generated within the chip, though for some reason known only to Ferranti they are not processed with mixed blanking, which is, however, available on the chip. Ferranti also generate the grey scale waveform upside down, i.e. it is a falling staircase, not a rising one as convention dictates. In order to keep the circuit as simple as possible this has not been changed, and its sense is unimportant for adjusting an amateur TV station.

The ZNA 234 requires a 2.5 MHz crystal oscillator, and all the electronics for this are within the chip. The crystal itself is connected between pins 8 and 9 and requires a small 22 pF capacitor in series with pin 8 (C1). The value of this capacitor can be varied to adjust the line speed of the generator.

The TV waveforms produced from the chip require 'holes' cut in them so as to accommodate the pulse information which is essential to a TV transmission in order to start the line and field scan generators of the receiver at the correct time. These gaps for the sync pulses are produced by a mixed (line and field) blanking signal which turn on the 1N914 diode and turns off TR1, so as to suppress the video signal.

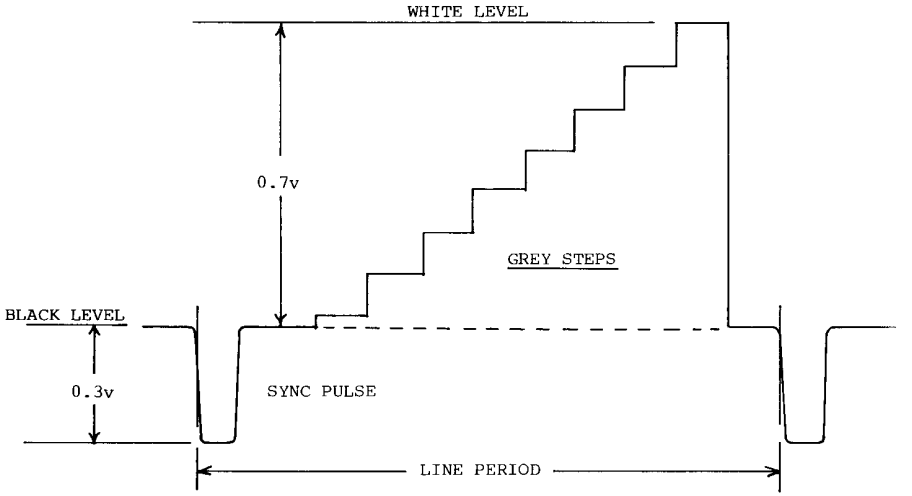
It would appear to follow from the circuit diagram that by turning off TR1 we would also turn off TR2, but things are not always what they seem; both pin 3 and pin 4 of the ZNA 234 are returned to the +5V rail by 3K3 resistors within the chip.

The next stage is to add sync pulses to the waveform. This is done by using the mixed sync output to turn TR2 off. You can do this by reducing its base potential below the limit set by the internal pull-up resistor on pin 3 and R3 R6 R7.



The sync pulses are narrower than the blanking pulses and are offset slightly to cause two holes in the picture, one before the sync pulse (called the front porch) and one after (back porch). The timings and levels of the various signals are shown, should an oscilloscope be available for viewing the signals. The output of TR2 is low impedance and a series resistor is included to restore the output impedance to 75 ohms. This output must be terminated in a 75 ohm resistor before measurements are taken. C2 C3 R4 and R5 are part of a low pass filter to stop any out of band transients reaching the video output. If the generator is required only for TV service work and not to drive a transmitter then they can be omitted.

IC2 is not essential to the working of the pattern generator, its purpose being to buffer the outputs and provide blanking and sync pulses at at standard level of 2V peak to peak when terminated in 75 ohms. These signals are useful for controlling other video equipment, but for a stand-alone pattern generator IC2 may be omitted.



BASIC GREY-SCALE WAVEFORM

PCB PROJECT

ELECTRONIC CAPTION WRITER

One use for the 2V mixed sync and blanking pulses is to drive an electronic character generator which gives you the ability to type 16 character messages superimposed on our test waveforms.

The 2V mixed sync pulses are fed into a window clip circuit which slices the centre section of the pulses and converts them into TTL level signals. The positive going edges of the sync pulses cause one half of a dual monostable to trigger for an unstable period given by its time constants 47K x 1n where C x R = 0.7T, i.e. about 33 microseconds. During the period when this monostable is unstable it allows the second half of the dual monostable to be triggered by a negative transition (this should happen only at the end of a frame scan when the equalising pulses are present).

At the end of the unstable period of the second monostable we start the character generator. The vertical position of the characters in the frame can be varied by adjusting the value of time constants associated with that monostable. The 47K resistor marked * can be decreased in order to move the characters up the screen.

Now we have positioned the characters on the TV frame we must consider how to generate them. Figure 2 shows a typical character, which is produced within the constraints of a matrix of 5 vertical columns and 9 horizontal rows. Producing the letters and figures is a 74S262AN integrated circuit. There are 128 characters available within the chip, each individual one being selected by a code supplied to connections B C D E F G H of the chip. The particular legend required is stored in memory elsewhere on our character generator board.

The horizontal direction of the character matrix is scanned by the column counter, which runs at 5 x 16 x line speed, i.e. 5 columns x 16 charcters for each line. After each of the five columns the generator is ready to receive the next character designation from the memory board; this information is carried on lines leading to pins J K L M (4 bit code, 16 locations). The 74S262AN supplies all five of its columns at the same time (parallel data). The column address is used to select one column at a time and this is handled by the 74151. The column counter is driven from a clock oscillator, which is synchronised to a feed of mixed blanking pulses.

The row selection is carried out within the 74S262AN. Pins 4 5 6 7 carry this code, which is derived from a row counter driven by the line rate pulses. Every four lines the character generator jumps to the next row.

The TTL signal corresponding to the characters is available at the output of the 74151 and is blanked and fed out via TR5.

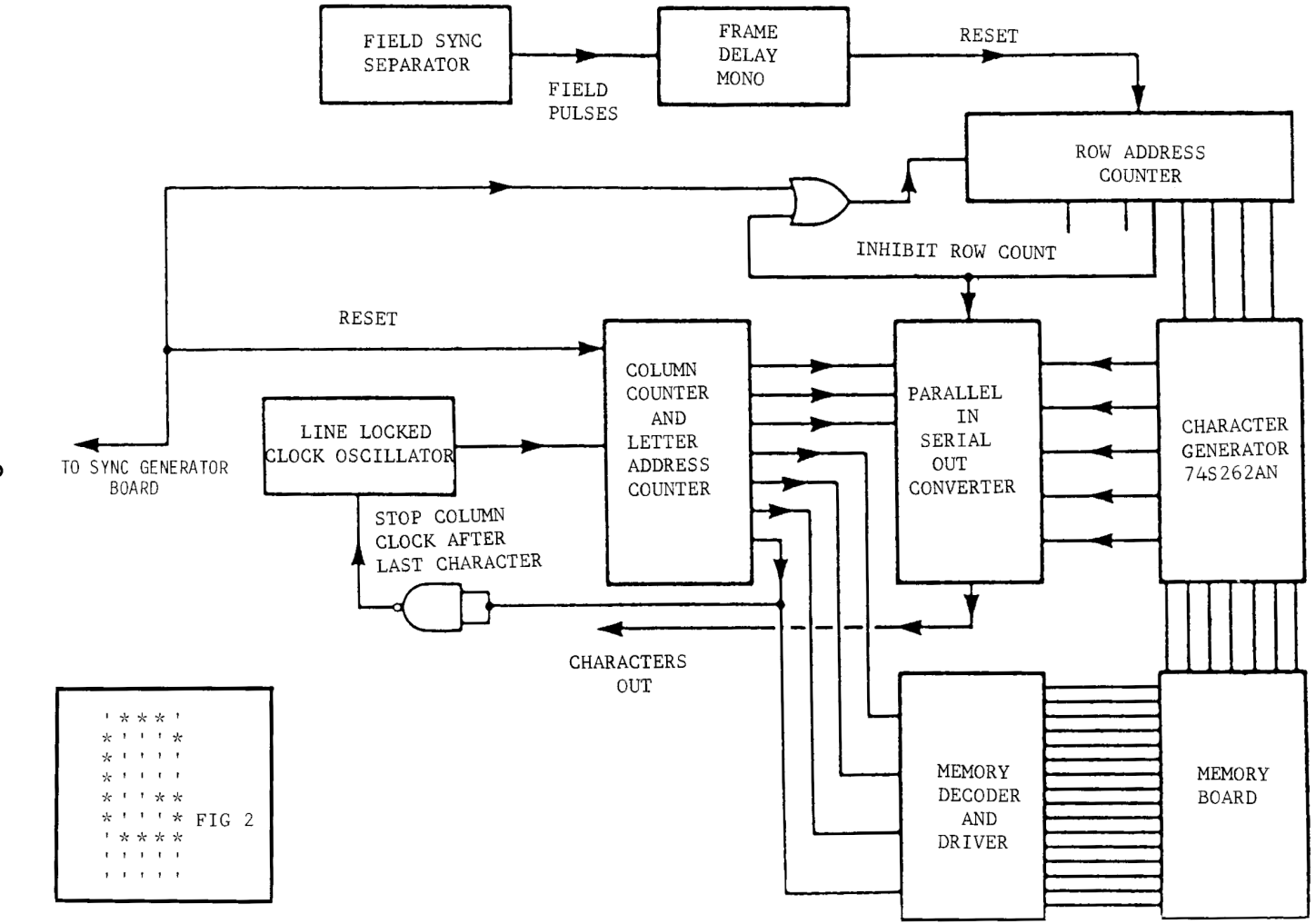
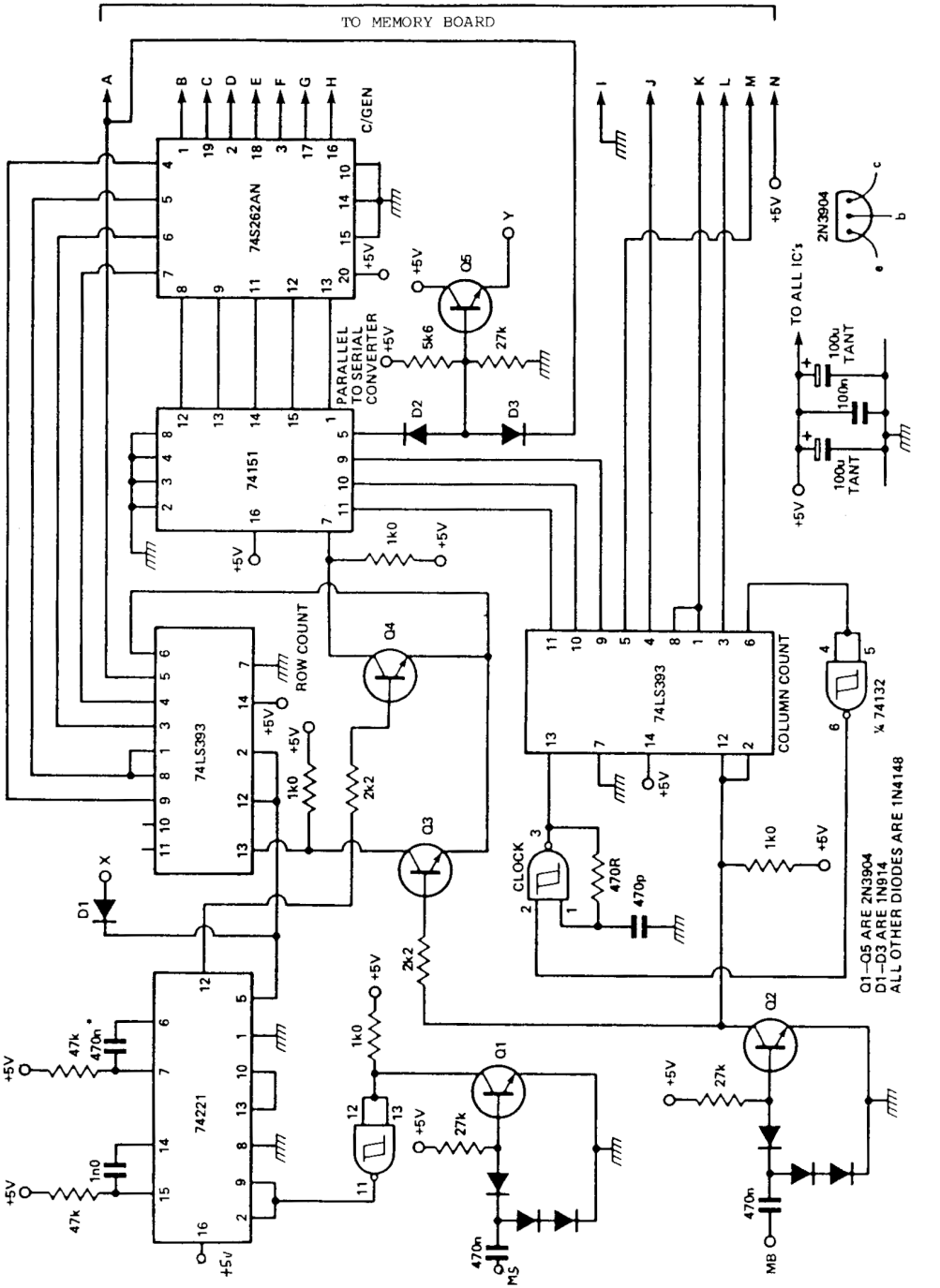
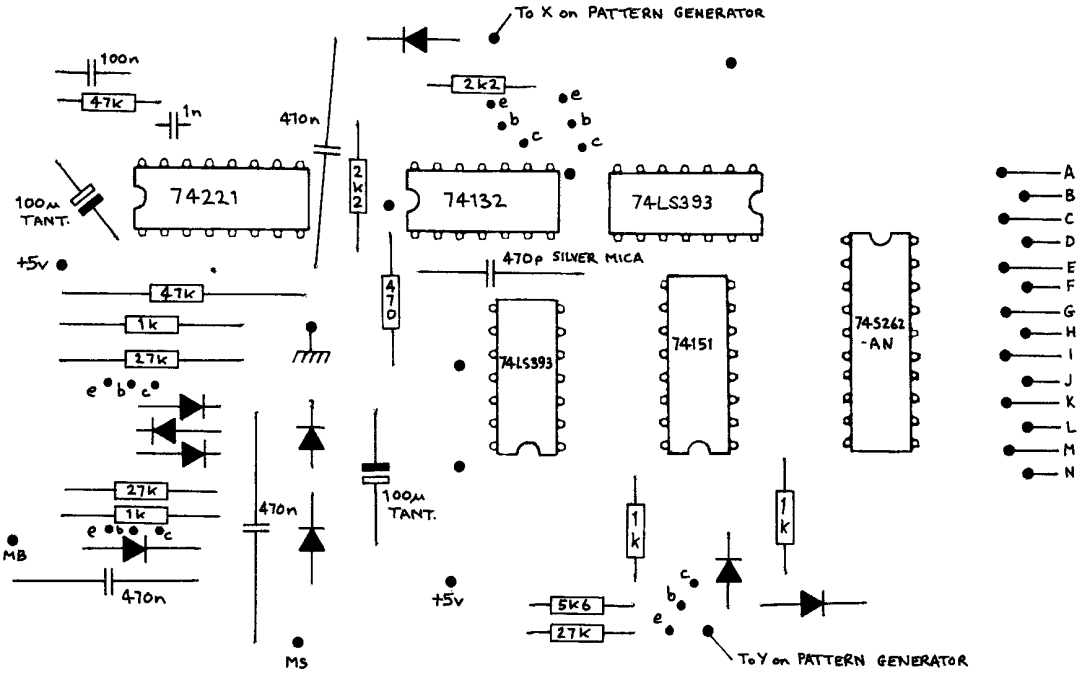
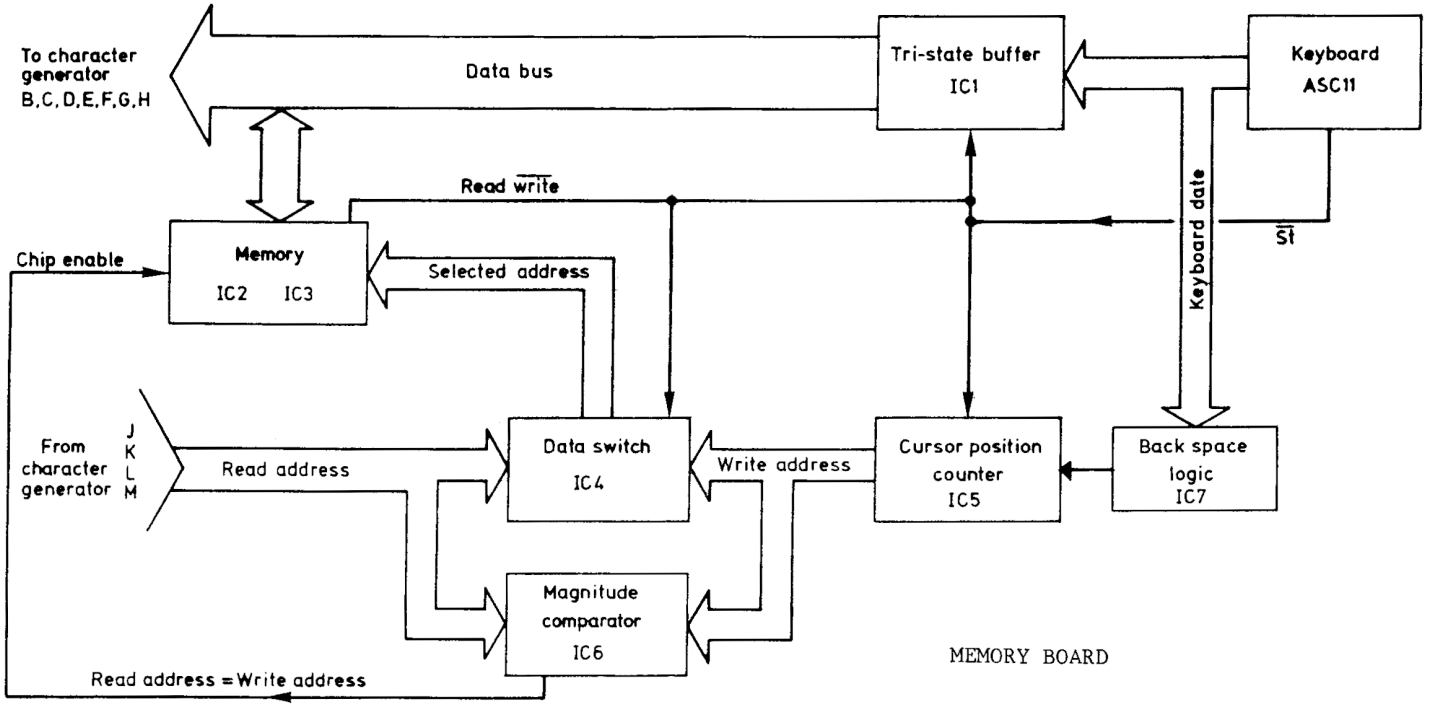

FIELD SYNC SEPARATOR
FIELD PULSES
FRAME DELAY MONO
RESET
ROW ADDRESS COUNTER
INHIBIT ROW COUNT
RESET
TO SYNC GENERATOR BOARD
LINE LOCKED CLOCK OSCILLATOR
STOP COLUMN CLOCK AFTER LAST CHARACTER
COLUMN COUNTER AND LETTER ADDRESS COUNTER
PARALLEL IN SERIAL OUT CONVERTER
CHARACTER GENERATOR 74S262AN
CHARACTERS OUT
MEMORY DECODER AND DRIVER
MEMORY BOARD

FIG 2


TO MEMORY BOARD
74S262AN
C/GEN
PARALLEL TO SERIAL CONVERTER
74151
74LS393
ROW COUNT
74LS393
COLUMN COUNT
74221
CLOCK
TO ALL IC's
2N3904
100u TANT
100n
5k6
27k
2k2
1k0
470R
470p
47k
470n
1n0
MS
MB
Q1–Q5 ARE 2N3904
D1–D3 ARE 1N914
ALL OTHER DIODES ARE 1N4148


To X on PATTERN GENERATOR
100n
47k
1n
470n
2k2
74221
74132
74LS393
100µ TANT.
+5v
470p SILVER MICA
47k
1k
27k
470
74LS393
74151
74S262 -AN
A
B
C
D
E
F
G
H
I
J
K
L
M
N
MB
470n
100µ TANT.
1k
1k
+5v
5k6
27k
To Y on PATTERN GENERATOR
MS


To character generator B,C,D,E,F,G,H
Data bus
Tri-state buffer IC1
Keyboard ASC11
Read write
Keyboard date
St
Chip enable
Memory IC2 IC3
Selected address
From character generator
J
K
L
M
Read address
Data switch IC4
Write address
Cursor position counter IC5
Back space logic IC7
Magnitude comparator IC6
Read address = Write address
MEMORY BOARD

MEMORY BOARD

The pins J K L M carry a four bit address code from the character generator which changes every time a different character is scanned. The information in that particular memory location is then available to the data bus.

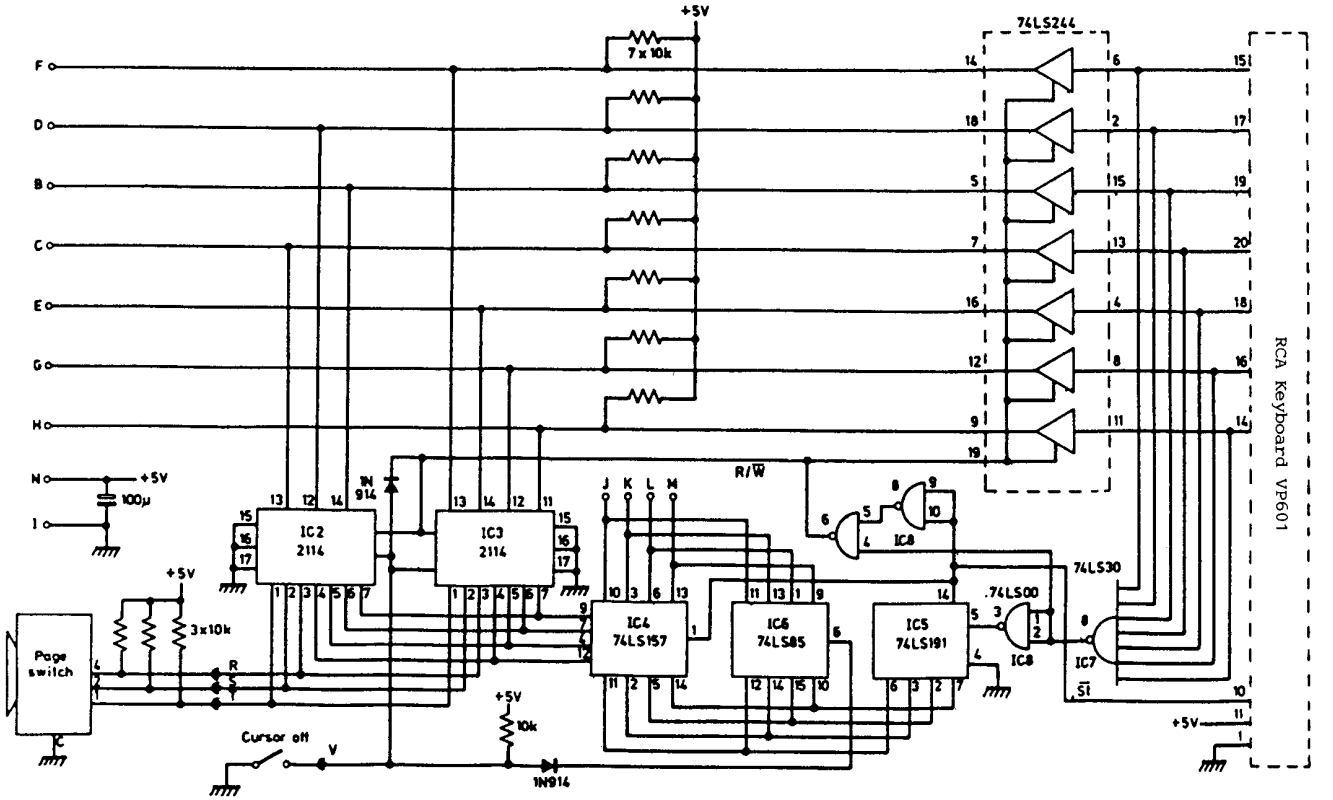
The next stage is to be able to determine the content of this memory, which is in fact RAM (random access memory). To do this we need to connect a keyboard to the data bus. An ASCII keyboard has seven data outputs and supplies a code to these outputs dependent on which key is pressed. The keyboard also provides a short pulse called the 'strobe' every time a key is pressed to indicate that the keyboard is sending data. This strobe pulse can be 'active high' or 'active low' and most keyboards provide both. Our circuit requires active low, designated ST with a line above the letters. When this signal occurs the outputs of IC1 (74S244), which are normally floating, assume the same state as the inputs and thus feed the keyboard output to the data bus. The stobe pulse also passes to the RAM where pin 10 of the memory chips (2114) is driven low. This puts them into a 'write' mode, enabling the data to be stored.

The next task is to control where the keyboard data is stored. By inserting IC4 in the address lines to the RAM we can switch these address lines in the write mode. IC4 (74S157) is a four bit data selector and functions just like a four pole double-throw switch, in that when pin 1 is driven low the RAM address lines are fed from the QA QB QC QD outputs of the counter chip IC5.

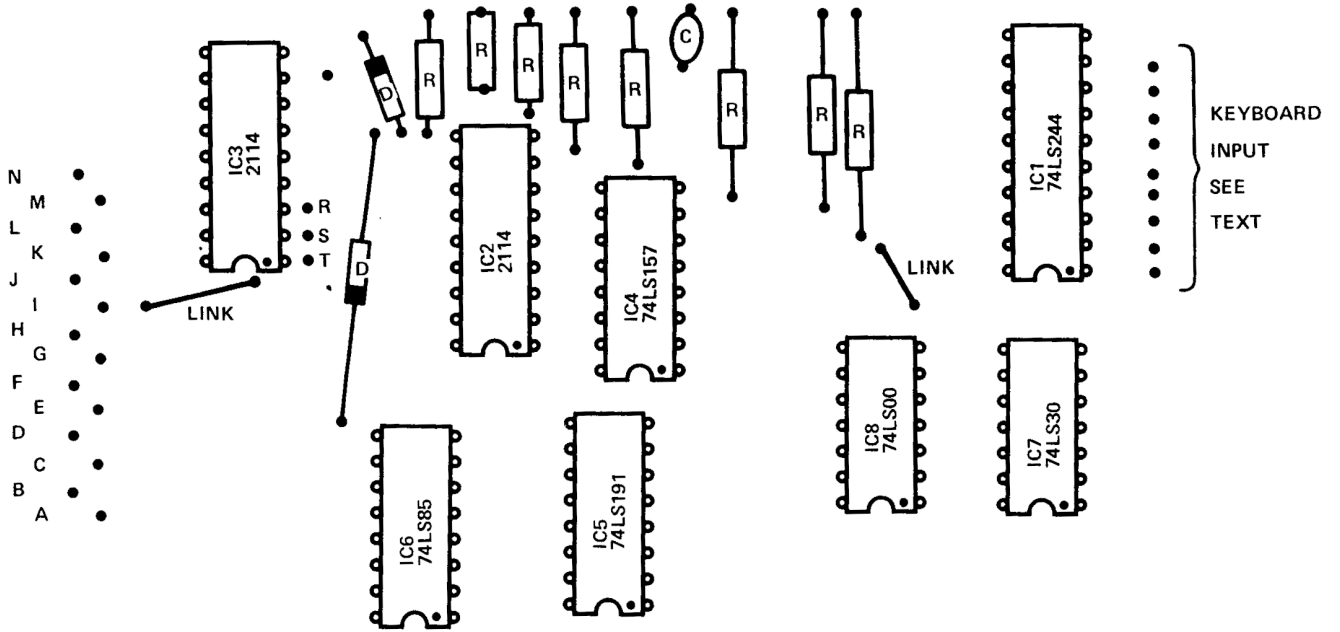
The write address is stored in IC5, a counter which counts up to 16 and then resets. By using the strobe pulse to advance it, its count will increase by one every time we press a key, ensuring that the selcted letter is stored in the next location in memory. When IC5 has been clocked to location 16 it will automatically reset to character location 1.

The next stage is to display a 'cursor' so that we can see the next location to be typed into on the screen. To do this we compare the read and write addresses in the four bit magnitude comparator IC6 (74LS85). When the two addresses are the same (i.e. the character generator is scanning the next location for typing) the output of the comparator, pin 6, goes high. This high state is connected to pin 8 of our RAM which is the chip enable pin (active low), so when our two addresses are identical the RAM is disabled. This causes the data bus to be pulled high by the 10K pull-up resistors and ensures that the data bus assumes a high state in the absence of data. If all the data bus bits are high then our caption writer will produce a white block, which makes an excellent cursor.

The full ASCII code provides many things besides letters and numbers, including cursor functions such as Backspace, Delete and Cursor Home. In order to keep this circuit simple these functions have not been decoded except code 7F (keyboard outputs 1111111 if you prefer): this is the Delete code. IC7 (74LS30) is an eight input NAND gate with seven of its inputs



MEMORY BOARD



MEMORY BOARD

ALL RESISTORS 10k
ALL DIODES 1N914
CAPACITOR 100u

looking at the keyboard output. Now when the delete code is presented by the keyboard the output of IC7 will be low. This signal is inverted and fed into the counter, with the following effect: when the counter is clocked by the strobe pulse it will count down instead of up. The output signal of IC7 is also used to inhibit the write signal to the RAM, so the cursor will step back and the information in the RAM will remain unchanged.

In effect we have created a backspace function, probably the most useful cursor function for a small character generator. The use of the Delete key for this function instead of the backspace key simplifies our circuit and does not cause too much operator confusion as keys like this are rarely used in a touch-type mode.

Switch S1 is used to remove the cursor; closing it inhibits the chip enable input of the RAM from going high, the state which generated the cursor. The page switch is optional and if not required pins 1 2 3 of the RAM should be connected to ground. Note that provision is not made on the PCB for the three 10K pull-up resistors associated with this switch. These are best fitted directly to the back of the switch.

All that remains is connecting up a keyboard, and on the prototype a RCA model CP601 was used. The output is via a PCB mounted socket, which takes a 3M connector no. 3421-6020. Pin numbers for this particular keyboard are shown on the circuit diagram. If you use another ASCII keyboard note that the strobe required is active low. Data lines are connected to pins 11 8 4 13 15 2 6 of the 74LS244 in that order, with pin 11 being the least significant bit.

PCB PROJECT

SIMPLE VISION SWITCHER

With the electronic vision switcher we can select which of any four video signals is routed to the transmitter. Our electronic test generator can be one of the sources, with a camera and home computer as other inputs.

Figure 1 shows the circuit of the switcher. The four video inputs are fed to the base of four single transistor amplifiers, all sharing a common 470 ohm load. The transistors are switched on and off at their emitters - to switch on any one of the four transistors we simply take its emitter down to logic zero. The video signal then present at its base will appear inverted across our common load resistor and pass to a two stage amplifier, where it is re-inverted and fed to the video output.

The logical zero states required at the emitter are supplied from an SN74139 IC. This chip will allow only one of its outputs to assume logic 0 at any one time. The 74139 is fed with a two wire logic signal from a push button selector.

Figure 2 shows a push button selector using momentary contact switches. The buttons are designated using a priority encoder, the information being retained in the 7475 latch. Figure 3 shows a simpler system using the mechanical latching type of press buttons.

The PCB layout is depicted in figure 4; the ground plane is on the component side. Only the circuitry of fig. 1 is assembled on the PCB as it is envisaged that the push button coder chips would be mounted adjacent to the switches.
The push button codes generated should be

Button one:	A logic 0, B logic 0.
Button two:	A logic 0, B logic 1.
Button three:	A logic 1, B logic 0.
Button four:	A logic 1, B logic 1.

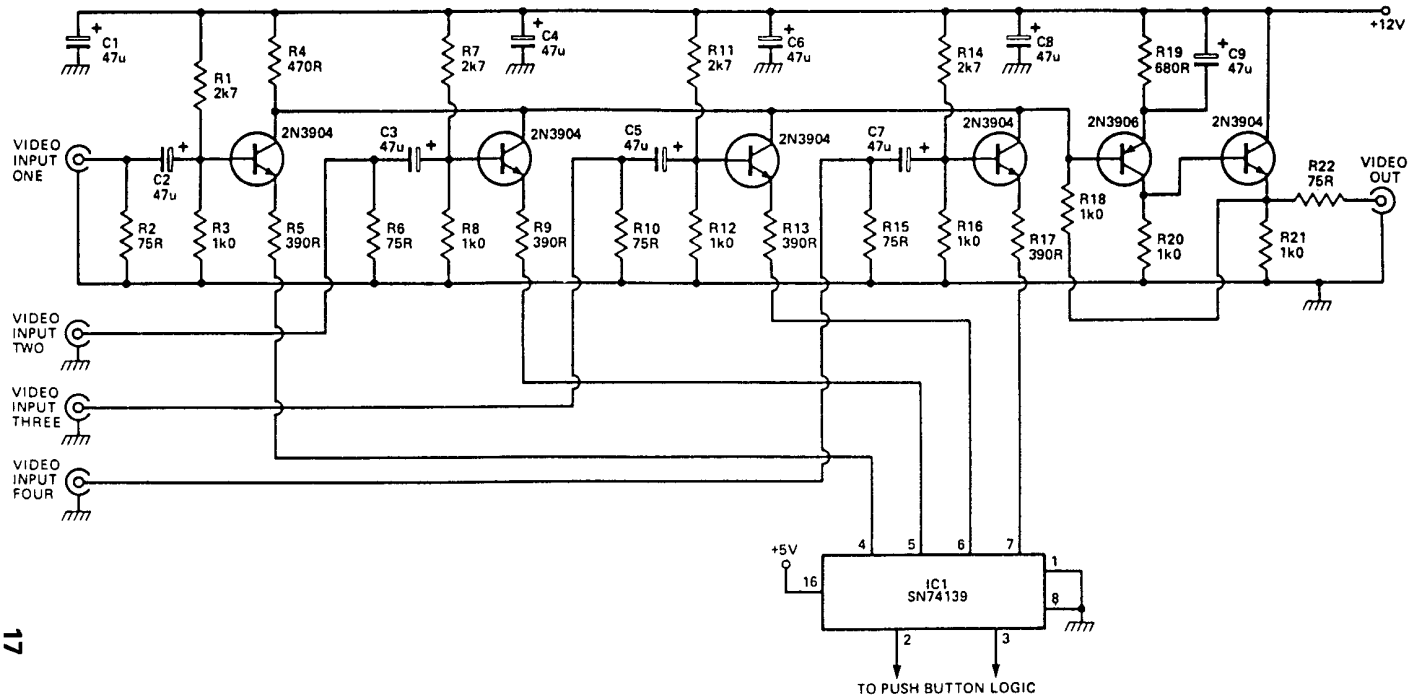
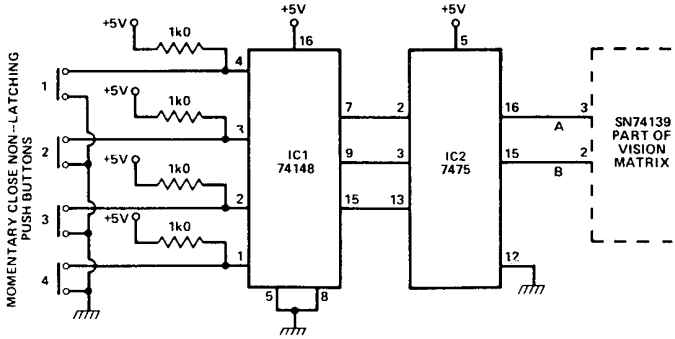
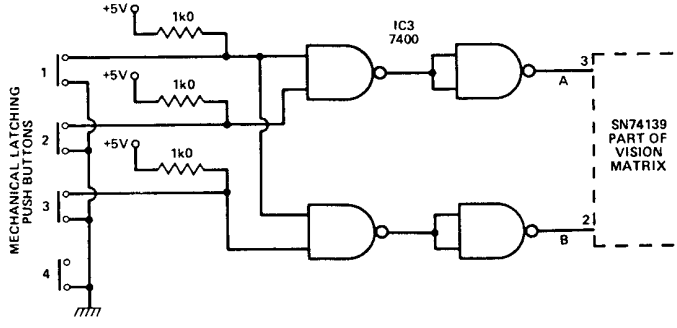


Fig.1 SWITCHER CIRCUIT DIAGRAM



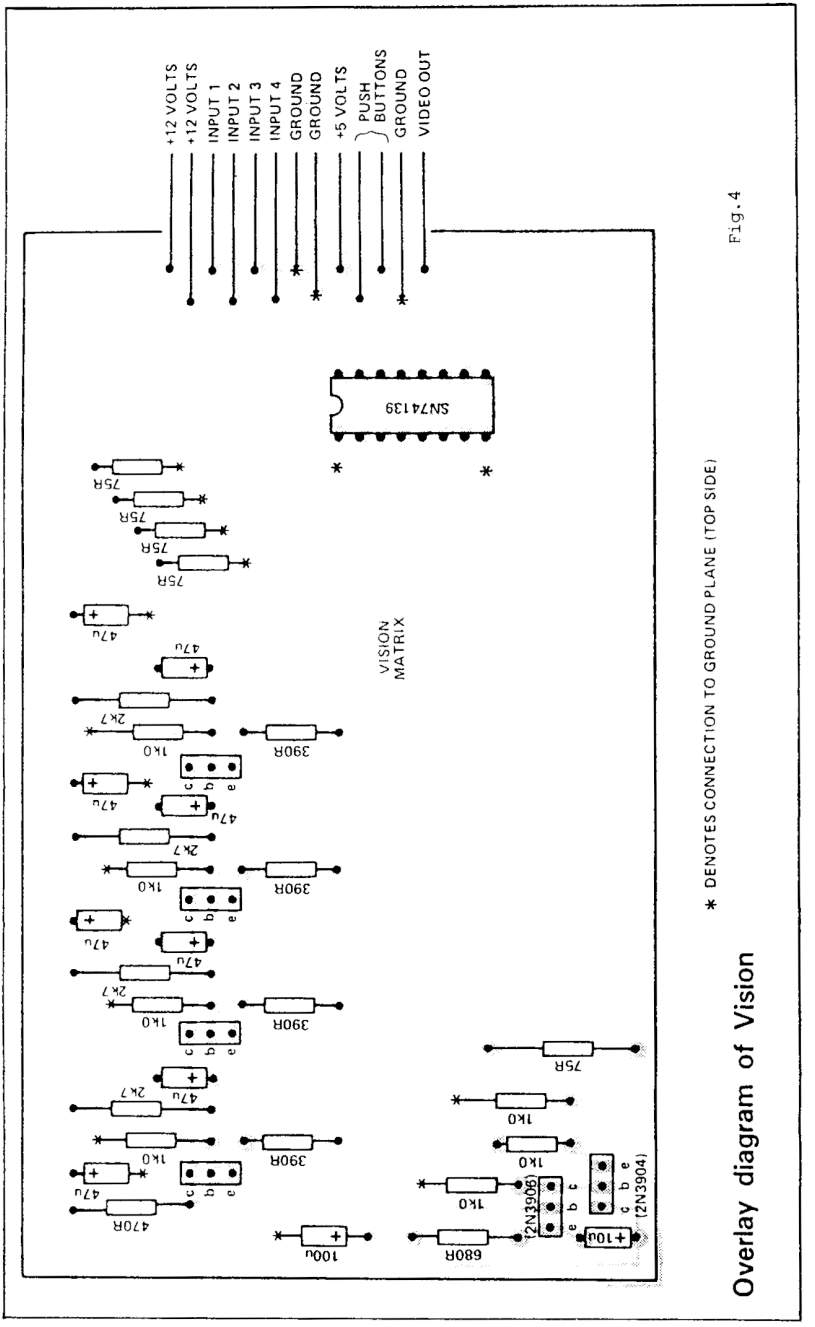
Push Button Selectors
(momentary contact)

Fig.2



Push Button Selectors
(mechanical latching)

Fig.3



* DENOTES CONNECTION TO GROUND PLANE (TOP SIDE)

Fig.4

Overlay diagram of Vision

CARD MODULE

CHAPTER 2
THE BEST OF THE HANDBOOKS

ELECTRONIC TESTCARD

INTRODUCTION

This unit was designed to provide an electronically generated test pattern to replace the conventional test-card/camera combination. The concept is not, of course, original; the familiar Philips PM5544 test card has been with us for some years now and many broadcasters have designed similar units for their own use. No particular merit for originality is claimed for this design except that it is simple and cheap enough for the average amateur to tackle.

FACILITIES

The generator requires an input of standard mixed-sync and mixed-blanking pulses plus a 5 volt power supply, and provides RGB outputs suitable for feeding to a colour encoder. The general appearance of the test card can be seen from the photograph although it is reproduced here in black and white. It is not as comprehensive as its commercial counterparts but does include the most important features needed for evaluation and adjustment of colour monitors, etc, these are as follows:

CROSSHATCH for linearity and convergence tests including a special central pattern for static convergence.
CASTELLATIONS for setting picture size.
A CIRCLE for aspect ratio and linearity tests.
GREY-SCALE and COLOUR BARS for video and coder adjustments.
MULTIBURST for focus and high frequency response.
LETTER BOX for low frequency response (smearing).
RED/WHITE alternate bars for testing chrominance/luminance delay.

In addition to the composite test card, individual full-screen waveforms can be selected by means of an optional thumbwheel switch.
These are:-

Field square-wave (50 Hz).
Multiburst (1.25 to 6.67 MHz).
Red/white bars.
Grey scale.
Colour bars (100%).
Peak white.
Black.
Line square-wave (15,625 Hz).
Cross-hatch (white on black).

Note that because of the masking effect of the circle, the multiburst part of the composite test card covers the frequency range 1.5 to 5 MHz.

GENERAL DESCRIPTION

The unit is split into three functional blocks, each of which occupies a standard sized, double sided printed circuit board.

Board-1 is the timing generator which accepts mixed syncs and blanking and generates a line-locked clock at approximately 40MHz (which is divided down to give various horizontal waveforms) and derives field and line drive pulses. This board also contains the circle generator which uses a PROM to store the circle shape information.

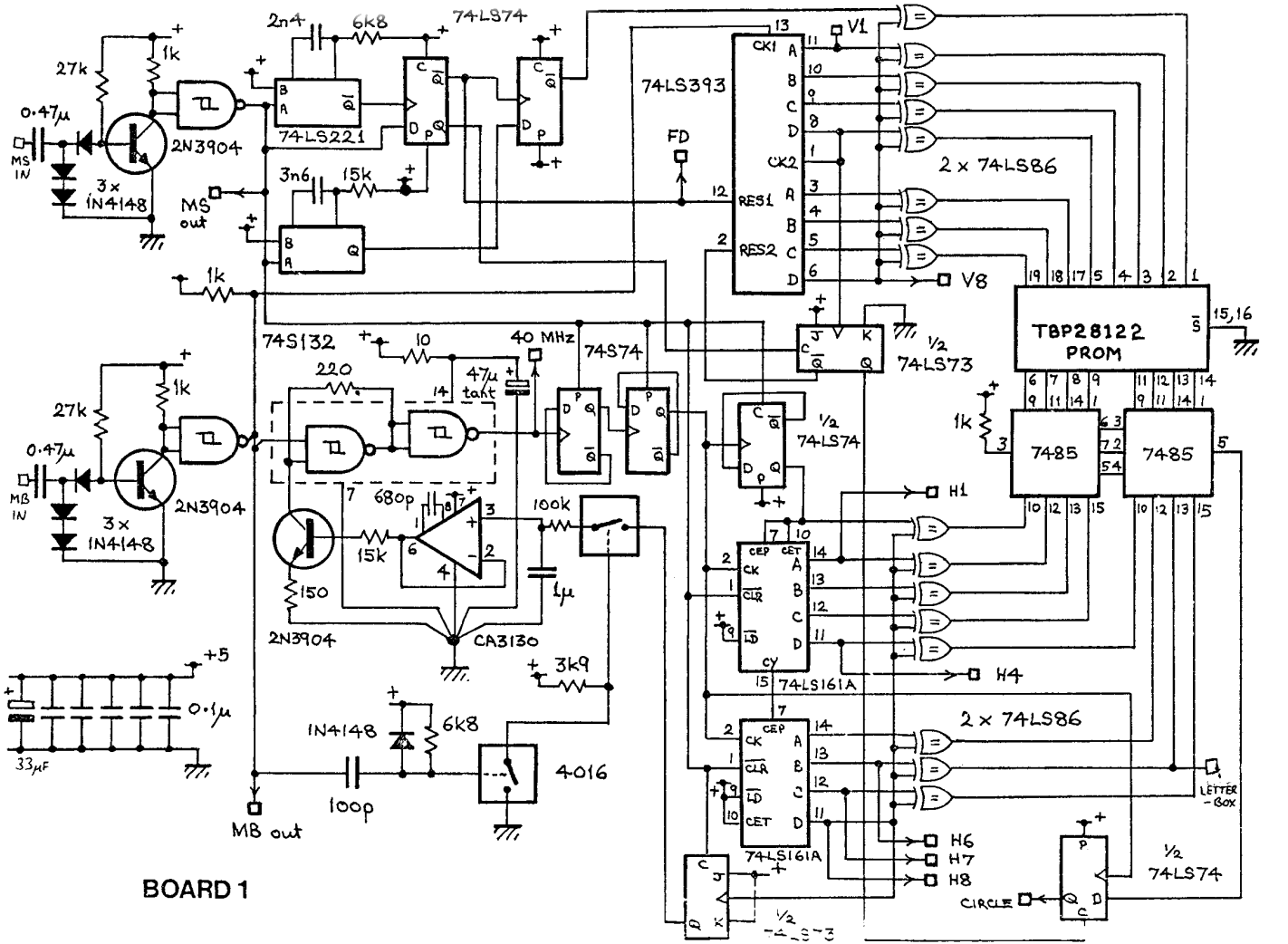
Board-2 generates the cross-hatch, multiburst and castellation waveforms by counting and gating together pulses from board 1: Board-3 combines and selects the various signals from the other two boards and produces the required RGB outputs. It would be a simple matter to adapt the final pattern to suit individual requirements, for example an electronically generated callsign could replace one of the patterns within the circle.

CICUIT DESCRIPTION - BOARD-1

The mixed sync and blanking inputs (standard 2v p-p) are first converted to TTL levels by the transistor and diode input circuits. The arrangement adopted results in the input signals being 'sliced' at a level of approximately twice the voltage dropped across a diode from their positive excursion, this being about right for 2v p-p pulses. If a non-standard pulse amplitude is used some experimentation may be required; any disturbance or glitches in the TTL syncs and blanking waveforms can wreak havoc in the digital circuitry.

The TTL sync signal is fed to two monostables, one with a period of approximately 11uS and the other 37uS, the output of the latter being a line frequency square-wave with half-line information removed. The output of the first monostable clocks a D-type flip-flop which has syncs fed to its D input, the result being that the Q output is normally 1 but during broad pulses it changes to 0, in other words, the output of the flip-flop is field drive. The field drive in turn clocks another D-type which this time has a 37uS monostable output fed to its D input. Because on one field the first broad pulse occurs during the first half of a line, and on the other during the second half, the flip-flop output consists of a 25Hz picture rate square wave.

The TTL mixed blanking signal enables a 40MHz oscillator consisting of a schmitt-trigger gate with feedback from output to input. A schottky device must be used here because a standard speed gate will not oscillate at 40MHz. It will be noticed that the usual capacitor from the schmitt input to ground is absent, and is replaced by a transistor! This transistor, along with stray capacitance allows the oscillator frequency to be varied so as to maintain the period of the oscillator at exactly one 2048th of the active line period (approx 52uS). Line locked oscillators are notoriously troublesome in their somewhat conflicting requirements of accurate frequency stability and precise phasing with respect to syncs. The novel approach adopted here is to separate these requirements by using a hard-gated oscillator to ensure good phase stability plus a slow-acting frequency control loop to keep their period correct. Obviously this does result in an oscillator which is sensitive to short term disturbance as is a free running oscillator, so extreme care must be taken not to couple noise or transient signals into it. In practice single

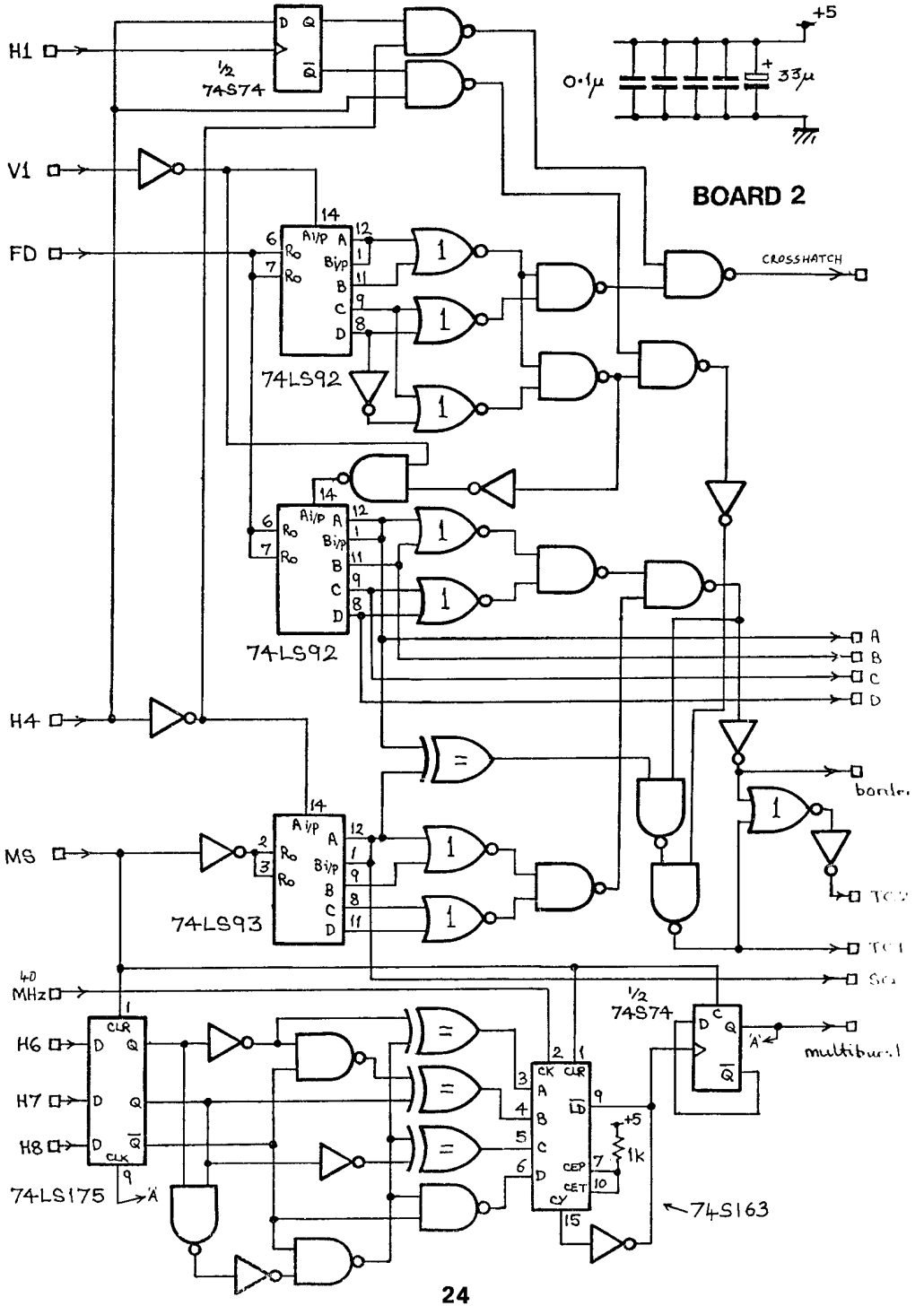

2n4
6k8
74LS74
27k
1k
0.47µ
MS IN
2N3904
3x 1N4148
74LS221
3n6
15k
MS out
74LS393
FD
V1
2 x 74LS86
V8
1k
74S132
10
40 MHz
74S74
220
47µ tant
TBP28122 PROM
15,16
1/2 74LS73
1/2 74LS74
MB IN
680p
100k
150
1µ
2N3904
CA3130
7485
7485
H1
H4
74LS161A
2 x 74LS86
LETTER-BOX
H6
H7
H8
CIRCLE
+5
0.1µ
33µF
1N4148
6k8
3k9
4016
100p
MB out
BOARD 1
22

point earthing has been found desirable plus local decoupling of the oscillator supply as shown on the circuit. It may be necessary to add a small capacitor (up to 10pF) from ground to the schmitt input.

The 40MHz clock is divided by 4 in the 74S74 to give a gated 10MHz clock (actually 9.86MHz) which feeds the horizontal counter. This consists of half of a dual D-type flip-flop plus two 4-bit synchronous counters, giving nine bits in all. The counter outputs follow a binary sequence of 0 to 511 from left to right across the television line. The most significant bit (MSB) of this counter is used to clock a J-K flip-flop on its negative transition. If the oscillator frequency becomes less than it should be there will be less than 512 clocks to the 9 bit counter during the active line period and the most significant bit will never be clocked back to zero. If however the frequency becomes high then the MSB will be clocked to zero before the end of the line. In the first case, therefore, the 74LS73 flip-flop output will remain low whereas in the second case it will be clocked high near the end of the TV line. The state of this flip-flop is sampled just at the beginning of the line blanking by means of the CMOS analogue switch (4016) and controls the charging/discharging of the 1uF capacitor. The voltage across this capacitor is monitored by the CA3130 FET input op-amp and determines the oscillator frequency. In this way the frequency is stabilised at the correct value. Several copies of this circuit have been made and it has been found to be very reliable.

The mixed blanking signal is also used to clock the 8-bit vertical (line) counter 74LS393. By means of the other half of the 74LS73 dual flip-flop, the most significant bits of this counter are held to zero until after the first sixteen lines following field blanking. As the number of active lines is 288 (which equals 256+32) this results in the vertical count of 0 to 255 being accurately centred in the picture. Because of the interlaced line structure, spacially adjacent lines are in fact in opposite fields. From a spacial point of view, therefore, the 25Hz picture square wave represents the least significant of the vertical sreen address, and is used as such. What we have then is a horizontal count and a vertical count, both running from 0 to 511, correctly centred in the active picture area. From these signals most of the waveforms needed for the test card can be derived.

The circle generator works on the principle of storing in a PROM the values of the horizontal co-ordinates of the edge of the circle for each TV line, that is it stores the values for X=SQR(RxR-YxY), one form of the equation of a circle of radius R. From what has been said, it might be thought that we need a value in the range 0 to 511 for each of 512 lines. However PROMs do not come with 9 bit outputs so it is fortunate that we can reduce this to 8 bits by taking advantage of the symmetry of the circle. The procedure adopted is to feed the 8 least signicant bits of both vertical and horizontal counts each into an exclusive-OR gate. The other inputs of the 8 vertical XOR gates are commoned and fed to the most significant bit of the vertical count and similarly the horizontal ones are connected to the most significant horizontal bit. In effect, we have arranged that counts 0 to 255 are unaffected (the XOR gates acting as non-inverting buffers) whereas counts 256 to 511 now become 255 to 0 on the exclusive-OR outputs because the 8 bits are inverted. We now have vertical and horizontal addresses which accurately reflect the symmetry of the circle and the PROM need hold only one quadrent's worth of data (256 eight bit words).


BOARD 2
H1
V1
FD
H4
MS
40 MHz
H6
H7
H8
1/2 74S74
74LS92
74LS92
74LS93
74LS175
74S163
0·1µ
33µ
+5
1k
CROSSHATCH
A
B
C
D
border
TC2
TC1
SC1
multibus-1

The modified vertical address is fed to the address inputs of the PROM, whose outputs now give the correct horizontal coordinate for the edges of the circle (note that the aspect ratio has been taken into account when calculating the PROM contents). All we need to do to actually generate the circle signal is to compare the PROM outputs with the modified (reflected) horizontal count; when the count exceeds the PROM data then we are inside the circle, otherwise we are outside! To this end, two 7485's are wired as an 8-bit comparator whose output is de-glitched by the remaining D-type flip-flop to provide a clean circle.

CROSSHATCH & CASTELLATION - BOARD-2

The waveforms produced on board 1 are not directly suitable for producing the crosshatch and castellation signals (which we will call the 'basic test-card') for two reasons; firstly we want the test-card squares to be truly square! Because of the aspect ratio, and the choice of horizontal clock frequency, a rectangle of say 16 lines by 16 clock pulses is not a square. With an aspect ratio of 4:3 we will get squares if we divide the screen into 16 (horizontal) x 12 (vertical) parts. We cannot easily derive the appropriate vertical waveform from the counter on board 1, so instead an additional divide-by-2 counter on board 2 is used clocked from the least significant output of the vertical counter on board 1 (shown as V1 on the circuit). This results in an overall division factor of 24 (12x24=288). The divide-by-16 horizontal waveform is already available on board 1 so what is the other problem? We want to produce an all-round castellation, but the size of the squares is too great to do this by having a central area of 10 by 14 squares and a one-square-thickness border all round. Rather,the ideal is to have a 15 by 11 central region with a half thickness border. This is what the second 74LS92 and the 74LS93 achieves. The arrangement adopted results in the second 74LS92 having a zero count during the top and bottom borders and the second 74LS93 having a zero count during the left and right borders. It is a simple matter to gate these signals together to produce a composite "border" signal. To make castellations, we must use this border signal to enable a "chequerboard" pattern - this is easily generated by gating together suitable horizontal and vertical square waves in an exclusive-OR gate (centre of circuit).

All that is now needed are two crosshatch patterns. One to form the dividing lines between the test-card squares (the lines are white and the squares grey) and the other two for the central static convergence pattern. It may not be obvious why two crosshatches are needed; for static convergence there must be a "cross" at dead centre, whereas the test-card one does not provide this - it is offset in both vertical and horizontal directions. The horizontal components of the two crosshatch patterns are derived by gating together the outputs of the first 74LS92, resulting in horizontals 4-lines (per picture) thick. The vertical components are obtained by means of the D-type flip-flop at the top of board 2 circuit diagram and when combined with the horizontals give the required crosshatch signals. The crosshatch which forms part of the "basic test card" is gated with the castellation and the border signals to form the component signals of the test-card (TC1 and TC2 on the circuit).

MULTIBURST - BOARD-2

The multiburst signal is derived by feeding the main 40MHz clock into a programmable divider whose division ratio is changed in eight steps across the active line. A square-wave output is required so the division factors must all be even. The factors chosen are:

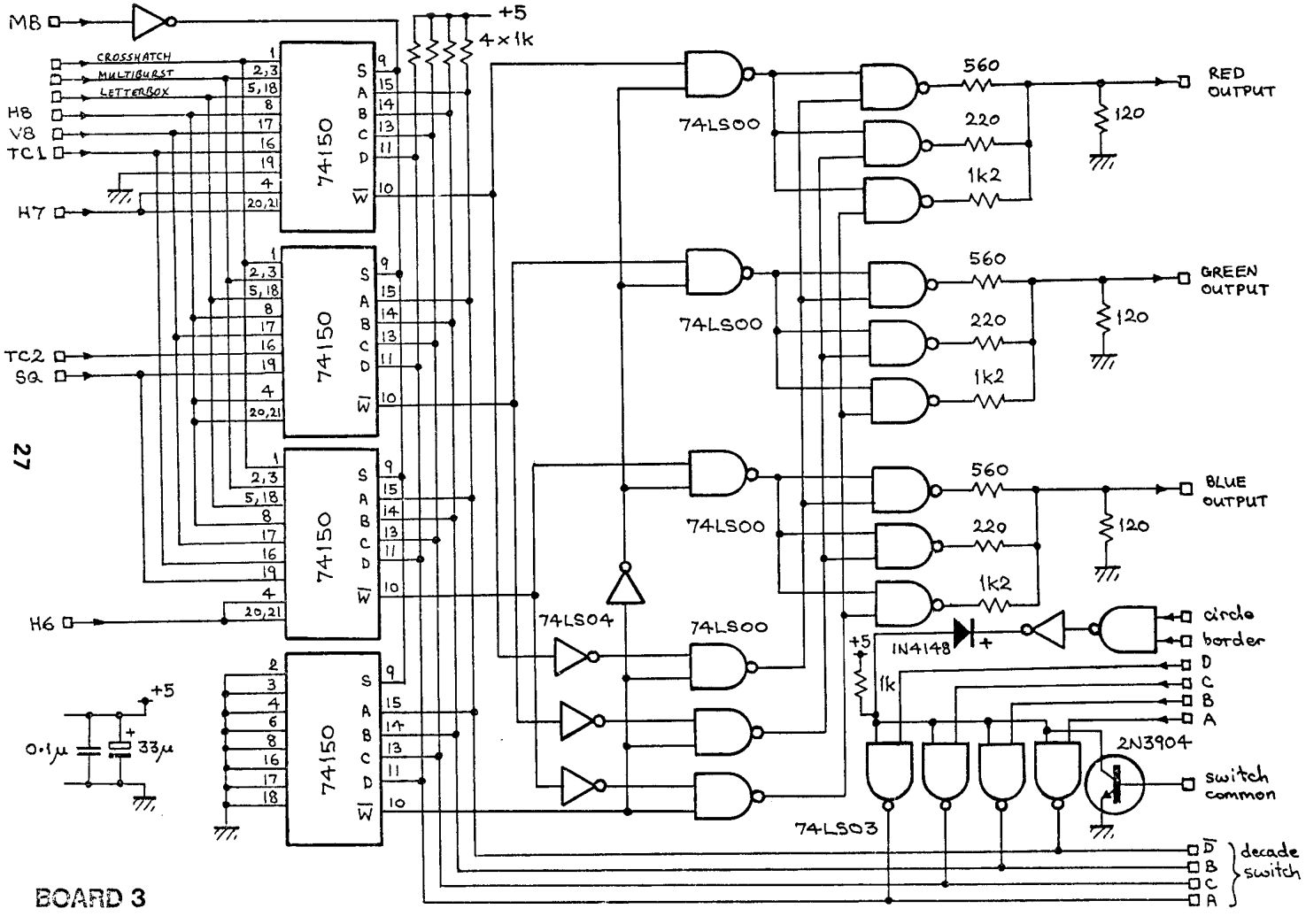
32	1.25 MHz
26	1.54 MHz
20	2.00 MHz
16	2.50 MHz
12	3.33 MHz
10	4.00 MHz
8	5.00 MHz
6	6.67 MHz

As mentioned earlier, the first and last are only available when the full-sreen multiburst is selected. A 3-bit horizontal address (H6, H7, H8) is taken from board 1 and latched by the 74LS175. It must then be converted into a four-bit code which, when fed to the preset inputs of the 74S163 divider, results in the required division ratios (in fact half the values given above because there is a subsequent divide-by-two stage). This is the function of the network of gates between the 74LS175 and the 74S163. If you care to work it out you should find that the correct code conversion is carried out, bearing in mind that the H8 output from the latch is inverted and that in fact the complement of the division ratio is required.

PATTERN SELECTOR & OUTPUT - BOARD-3

This board has the simple job of selecting the required patterns to the correct parts of the screen, and of providing the RGB outputs. There are fourteen possible combinations of outputs - eight luminance values, from black through grey to white (R=G=B), plus the six saturated colours obtainable from the primaries (red, green, blue, yellow, cyan, magenta). The output stages consist of TTL stages resistively matrixed together so that each output, when terminated in 75-ohms, can take up a voltage between 0v and 0.7v in steps of 0.1v. The output circuitry is fed from four TTL lines; one selects monochrome or colour and the other three select either one of eight luminance values or one of the colours. Both black and white are obtainable either when "monochrome" or "colour" is selected, and advantage is taken of this to slightly simplify the selection circuitry.

The four bits controlling the output stages are fed from four 16 to 1 line multiplexers (74150) which have the various pattern signals from boards 1 and 2 fed to their inputs. When a full-screen pattern is selected the thumbwheel switch data is simply fed to the multiplexer address inputs. The circuit is arranged so that, using a decade thumbwheel having true and inverted outputs wired as shown, positions 0.through 7 and 9 select the nine patterns listed earlier. When the switch is at position 8, the common becomes open circuit and the 2N3904 turns off, thus allowing the A-D vertical select lines (from board 2) to control the multiplexers when the circle signal corresponds to "inside". When the circle is set at 0 ("outside") the multiplexers receive an address of 1111 which selects the "basic test card" to the outputs, the result being the full test-card display as shown in the photogragh. By re-arranging the inputs


MB
CROSSHATCH
MULTIBURST
LETTERBOX
H8
V8
TC1
H7
TC2
SQ
H6
+5
4×1k
74150
74LS00
74LS04
74LS03
560
220
1k2
120
RED OUTPUT
GREEN OUTPUT
BLUE OUTPUT
IN4148
circle
border
D
C
B
A
2N3904
switch common
decade switch
0.1µ
33µ
1k
BOARD 3
27

to the 74150's many different effects can be achieved, but bear in mind that some inputs are used only in the test-card (e.g. letter box) and others only for full screen patterns (e.g. field square wave V8).

CONSTRUCTION & TESTING

A set of three double-sided printed circuit boards, as well as a pre-programmed PROM, are available from BATC 'Members Services'. The current issue of CQ-TV magazine should be consulted for details.

The boards come complete with layout diagrams which should be followed carefully. Experience has shown, now that a great many test cards have been built, that in almost every case where trouble is experienced, the constructor has failed to solder those components which act as 'through stakes' for the board, on BOTH sides. If trouble is encountered it is strongly recommended that a very thorough examination of the solder points be made.

No serious problems should be encountered in getting the generator to work as long as good high-speed logic construction techniques are adopted throughout. Take particular care with decoupling and earthing. Trouble spots, if any, are likely to be the 40MHz oscillator on board 1 and the multiburst divider on board 2. Feeding a 40MHz TTL signal along more than an inch or two of wire can be tricky, and you may find it helps to add a small series resistor at the sending end to absorb reflections.

A useful tip is to temporarily disconnect one of the pattern inputs to board 3 and instead connect a flying lead to the 74150. If you select this input with the switch, you have a ready made probe which can be used to monitor signals within the generator on a TV screen. Mixed line and field rate signals, meaningless on an oscilloscope, are made instantly recognisable by this method.

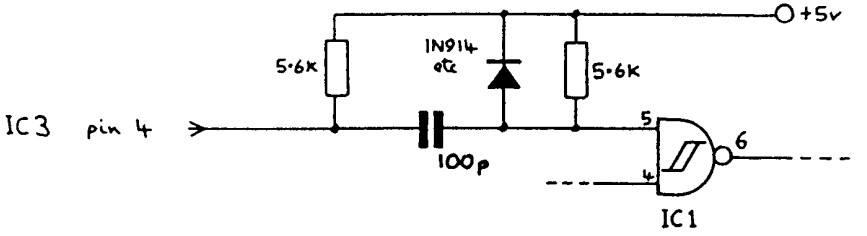
TBP28122 PROM for test-card generator.

(Hexadecimal notation)

0000	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0010	F0	EA	E6	E2	DF	DB	D9	D6	D4	D1	CF	CD	CB	C9	C7	C6
0020	C4	C2	C1	BF	BE	BC	BB	B9	B8	B7	B5	B4	B3	B2	B0	AF
0030	AE	AD	AC	AB	AA	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	9F
0040	9E	9D	9C	9C	9B	9A	99	98	97	97	96	95	94	94	93	92
0050	92	91	90	8F	8F	8E	8D	8D	8C	8B	8B	8A	8A	89	88	88
0060	87	87	86	85	85	84	84	83	83	82	82	81	81	80	80	7F
0070	7F	7E	7E	7D	7D	7C	7C	7B	7B	7A	7A	79	79	79	78	78
0080	77	77	76	76	76	75	75	74	74	74	73	73	73	72	72	71
0090	71	71	70	70	70	6F	6F	6F	6E	6E	6E	6E	6D	6D	6D	6C
00A0	6C	6C	6C	6B	6B	6B	6A	6A	6A	6A	69	69	69	69	68	68
00B0	68	68	67	67	67	67	67	66	66	66	66	66	65	65	65	65
00C0	65	64	64	64	64	64	64	63	63	63	63	63	63	63	62	62
00D0	62	62	62	62	62	61	61	61	61	61	61	61	61	61	61	60
00E0	60	60	60	60	60	60	60	60	60	60	60	60	60	5F	5F	5F
00F0	5F	5F	5F	5F	5F	5F	5F	5F	5F	5F	5F	5F	5F	5F	5F	5F

ADDENDUM

Since this circuit first appeared in BATC handbook-1, John Sager G8OHN, noticing a small jitter problem associated with the multiburst signal, found that by applying a clock pulse to IC19 during the reset pulse an improvement could be affected. The following circuit may be used to accomplish this although some modification to the PC boards are necessary.



Break the track between Pins 4 & 5 of IC1 (board-1) and wire in the components as shown, this generates a pulse on the 40MHz clock line shortly after the begining of the line sync pulse to reset IC19.

The jitter problem is caused because the 74S163 in the original cicuit is never reset, and the counter is left with one of the three consecutive counts from the previous line, which vary randomly due to the operation of the phase lock circuit for the 40MHz oscillator. Thus the multiburst can start 25nS early or late.

TEST CARD PARTS LIST.

BOARD-1

2 off 7485
1 off 74LS73
2 off 74LS74
4 off 74LS86
2 off 74LS161A
1 off 74LS221
1 off 74LS393
1 off 74S74
1 off 74S132
1 off TBP28122 (PROM)
1 off CD4016
1 off CA3130

3 off 2N3904
7 off 1N4148

2 off 0.47uF polyester
1 off 1uF polyester
1 off 2n4 polystyrene
1 off 3n6 polystyrene
1 off 680pF polystyrene
1 off 100pF ceramic
5 off 100nF ceramic disc
1 off 33uF 6.3v electrolytic
1 off 47uF 6.3v tantalum

1 off 10 ohm
1 Off 150 ohm
1 off 220 ohm
2 off 1K
1 off 3.9K
2 off 6.8K
2 off 15K
2 off 27K
1 off 100K
all resistors ¼W

BOARD-2

4 off 74LS00
2 off 74LS02
2 off 74LS04
1 off 74LS86
2 off 74LS92
1 off 74LS93
1 off 74LS175
1 off 74S74
1 off 74S163

4 off 100n ceramic disc
1 off 33uF 6.3v electrolytic

1 off 1K ¼W

BOARD 3

4 off 74LS00
1 off 74LS03
1 off 74LS04
4 off 74150

1 off 2N3904
1 off 1N4148

1 off 100n ceramic disc
1 off 33uF 6.3v elecrolytic

3 off 120 ohm
3 off 220 ohm
3 off 560 ohm
5 off 1K
3 off 1.2K
all resistors ¼W

CARD MODULE

PAL CODER

This encoder takes the basic red, green and blue colour signals and combines them with syncs and other necessary signals to produce a composite PAL colour video signal.

The unit has been made as simple as possible and features a single IC balanced modulator circuit, no complicated filter networks to adjust thus avoiding the need for luminance delay, single PC board, simple adjustment, single power supply requirements and low cost. This simplicity means that the residual carrier balance is outside professional broadcast standards though this is of little consequence to the amateur, and there is no bandwidth limiting of the chroma information. The harmonics of the colour sub-carrier frequency however have been reduced to acceptable levels with a simple filter.

SPECIFICATION

INPUTS.	a.	Standard 0.7v non-composite RGB into 75 ohms.
	b.	Colour sub-carrier (CRC), 0.5 - 1v p-p into 75 ohms. frequency 4.433 MHz.
OUTPUT.		1v p-p composite video across 75 ohms.
POWER SUPPLY.		10 - 12v dc stabilized.

DESCRIPTION

A block diagram of the PAL coder is shown in Fig 1. The coder uses a low-cost TV receiver decoder integrated circuit (IC1) in the "reverse" direction to code B-Y and R-Y signals into PAL video. The coder is a linear as opposed to a digital device and may be used for coding normal video signals from a camera, flying-spot scanner etc., as well as those from digital sources.

Red, green and blue video input signals are matrixed along with a burst gate pulse to give B-Y, R-Y and luminance signals as well as colour burst. Processing is done by TR1, 2 and 3 and associated resistor networks.

The B-Y and R-Y signals are a.c. coupled and need to be referred to a d.c. level before entering the balanced modulator IC1. Buffering and clamping, using mixed syncs, is carried out by TR4, 5, 6 and 7 for the B-Y signal channel and by TR8, 9, 10 and 11 for the R-Y channel.

IC1 accepts B-Y and R-Y signals, colour sub-carrier quadrature signals and axis switch (alternate line) signals. The output from IC1 consists of a full bandwidth PAL coded chrominance signal.

The last section of the coder adds the chrominance and luminance signals, together with the mixed sync signals, to provide a composite PAL coded signal at standard level. Gain setting and output stage are provided by TR12, 13 and 14.

It should be noted that in the interests of simplicity the colour signals exist at full bandwidth. A simple low Q filter is included between the modulator and the output amplifier to reduce the harmonic content to an acceptable level.

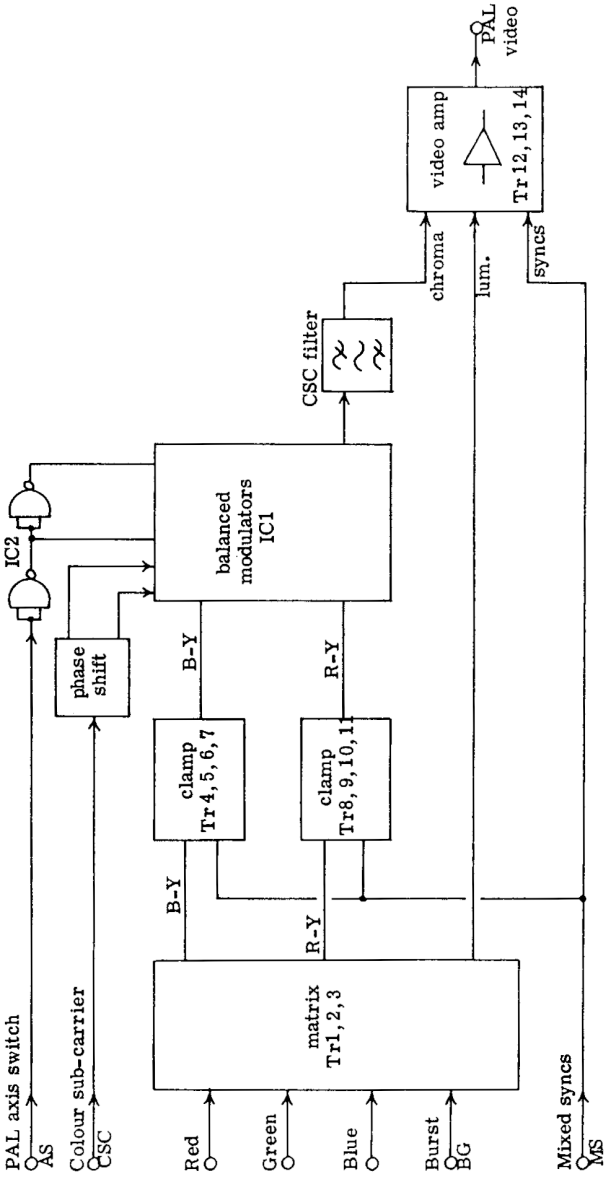
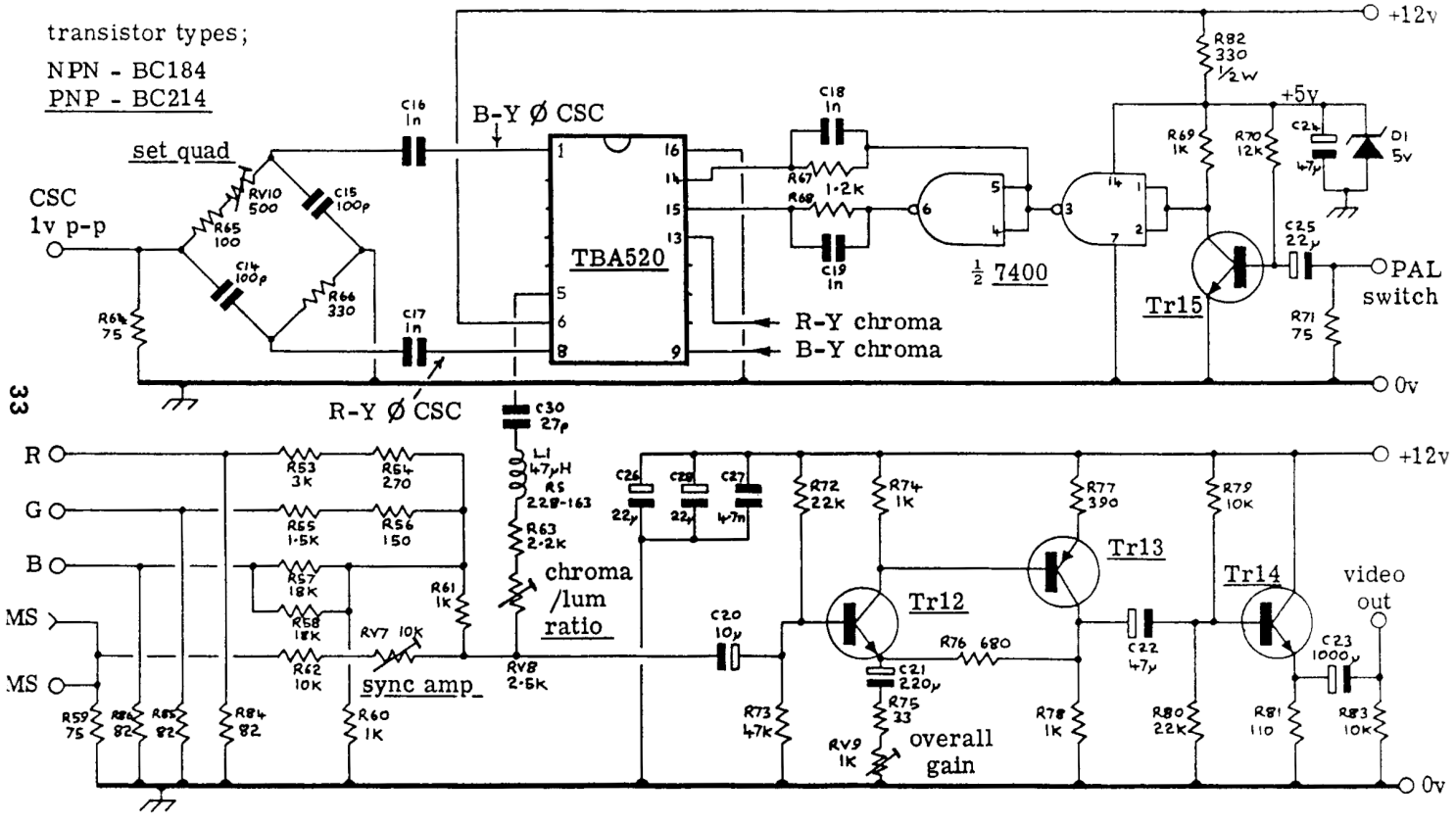
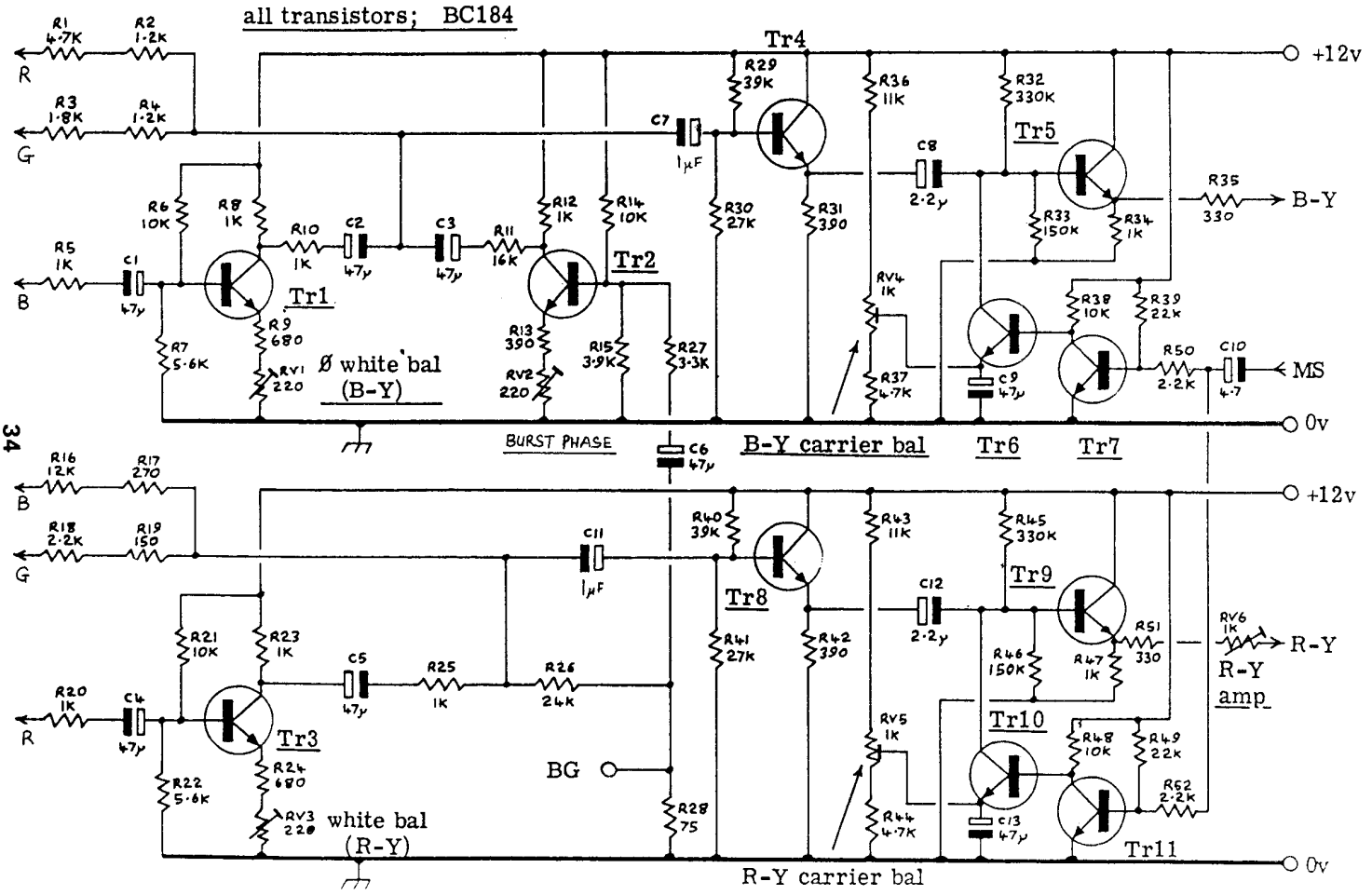


Fig.1. PAL CODER BLOCK DIAGRAM.


transistor types;
NPN - BC184
PNP - BC214
set quad
CSC
1v p-p
B-Y Ø CSC
R-Y Ø CSC
TBA520
R-Y chroma
B-Y chroma
½ 7400
Tr15
PAL
switch
+12v
+5v
0v
chroma
/lum
ratio
sync amp
overall
gain
Tr12
Tr13
Tr14
video
out
R
G
B
MS
MS


all transistors; BC184
R1 4·7K
R2 1·2K
R
R3 1·8K
R4 1·2K
G
B
R5 1K
C1 47μ
R6 10K
R8 1K
R10 1K
C2 47μ
C3 47μ
R11 16K
R12 1K
R14 10K
Tr1
R9 680
R7 5·6K
RV1 220
Ø white bal (B-Y)
Tr2
R13 390
RV2 220
R15 3·9K
R27 3·3K
Tr4
R29 39K
C7 1μF
R30 27K
R31 390
R36 11K
RV4 1K
R37 4·7K
C8 2·2μ
R32 330K
Tr5
R33 150K
R34 1K
R35 330
B-Y
+12v
R38 10K
R39 22K
C9 47μ
R50 2·2K
C10 4·7
MS
0v
BURST PHASE
C6 47μ
B-Y carrier bal
Tr6
Tr7
34
R16 12K
R17 270
B
R18 2·2K
R19 150
G
C11 1μF
R40 39K
Tr8
R41 27K
R42 390
R43 11K
C12 2·2μ
R45 330K
Tr9
R46 150K
R47 1K
R51 330
RV6 1K
R-Y
R-Y amp
+12v
R21 10K
R23 1K
C5 47μ
R25 1K
R26 24K
R20 1K
C4 47μ
R
Tr3
R22 5·6K
R24 680
RV3 220
white bal (R-Y)
BG
R28 75
RV5 1K
R44 4·7K
Tr10
R48 10K
R49 22K
C13 47μ
R52 2·2K
Tr11
R-Y carrier bal
0v

The PAL coder has been tested on colour bars and colour signals from a studio camera and gives very acceptable results on a vectorscope and subjectively when compared with a professional coder costing several thousand pounds!

CONSTRUCTION

The coder is built on a single sided PC board measuring 114 x 203mm, with connections brought out to the edge of the board making it suitable for plugging into a direct edge connector (0.1" spacing). The printed circuit board is available from BATC 'Members Services' department, details of which are to be found in the current issue of CQ-TV magazine.

In its original form, the TBA520 (IC1) was in the suffix 'Q' (QIL) version and had physically "staggered" pins. These should be carefully bent with pointed nosed pliers to convert it into a "dual inline" device. DIL sockets should be fitted for both IC1 and IC2.

SETTING-UP PROCEDURE

Setting up should preferably be done using an oscilloscope connected to the output although an alternative method using a colour monitor is also given.

Since the carrier balance is voltage sensitive it should be set up with the power supply which will be used in the finihed unit.

PROCEDURE

1. No input to R,G,B. Terminate output with a 75-ohm resistor.

   Scope. Adjust CARRIER BAL RV4 and RV5 for minimum colour sub-carrier.
   Mon/TV. Increase COLOUR SATURATION on monitor,
   adjust RV4 for minimum blue/yellow tinting,
   adjust RV5 for minimum red/cyan tinting,
   repeat until neutral background is obtained.

2. Colour Bars to R.G.B. inputs. Short inputs together.

   Scope. Adjust WHITE BAL RV1 AND RV3 for minimum colour sub-carrier.
   Mon/TV. Adjust WHITE BAL RV1 to minimise blue/yellow tint,
   adjust WHITE BAL RV3 to minimise red/cyan tint.

3. Remove R.G.B. short.

   Scope. Adjust QUAD RV10 for minimum "twitter" on waveform when viewed at line rate with scope trigger control adjusted for "twitter" effect between alternate lines.
   Mon/TV. Adjust QUAD RV10 for best saturation (look at red or blue bar).

4. Chrominance/luminance levels.

   Scope. Adjust R-Y AMP RV6 for top of cyan bar envelope to equal top of yellow bar.
   Adjust CHROMA/LUM RV8 for bottom of green bar to sit at black level.
   Mon/TV. Switch off R and G guns of monitor,

adjust CHROMA/LUM RV8 for equal brightness of blue in white bar and blue bar positions.
Switch off B gun, switch on R gun,
Adjust R-Y AMP RV6 for equal red intensity in white bar and red bar positions.Return monitor to normal working.

TV. First adjust saturation using normal off-air pictures, preferably colour bars. (bear in mind that there are 95% bars (BBC) or EBU bars (ITV).
Adjust as for monitor.

5. Overall gain and sync amplitude.

Scope. Adjust SET OVERALL GAIN RV9 for 0.7v p-p video only, (ignoring sync amplitude).
Adjust SYNC AMP RV7 for 0.3v p-p sync, giving 1v p-p composite video.

Mon/TV. Set SYNC AMP RV7 to mid-position,
adjust SET OVERALL GAIN RV9 for maximum contrast consistent with no sign of clipping (colour changes in yellow bar).

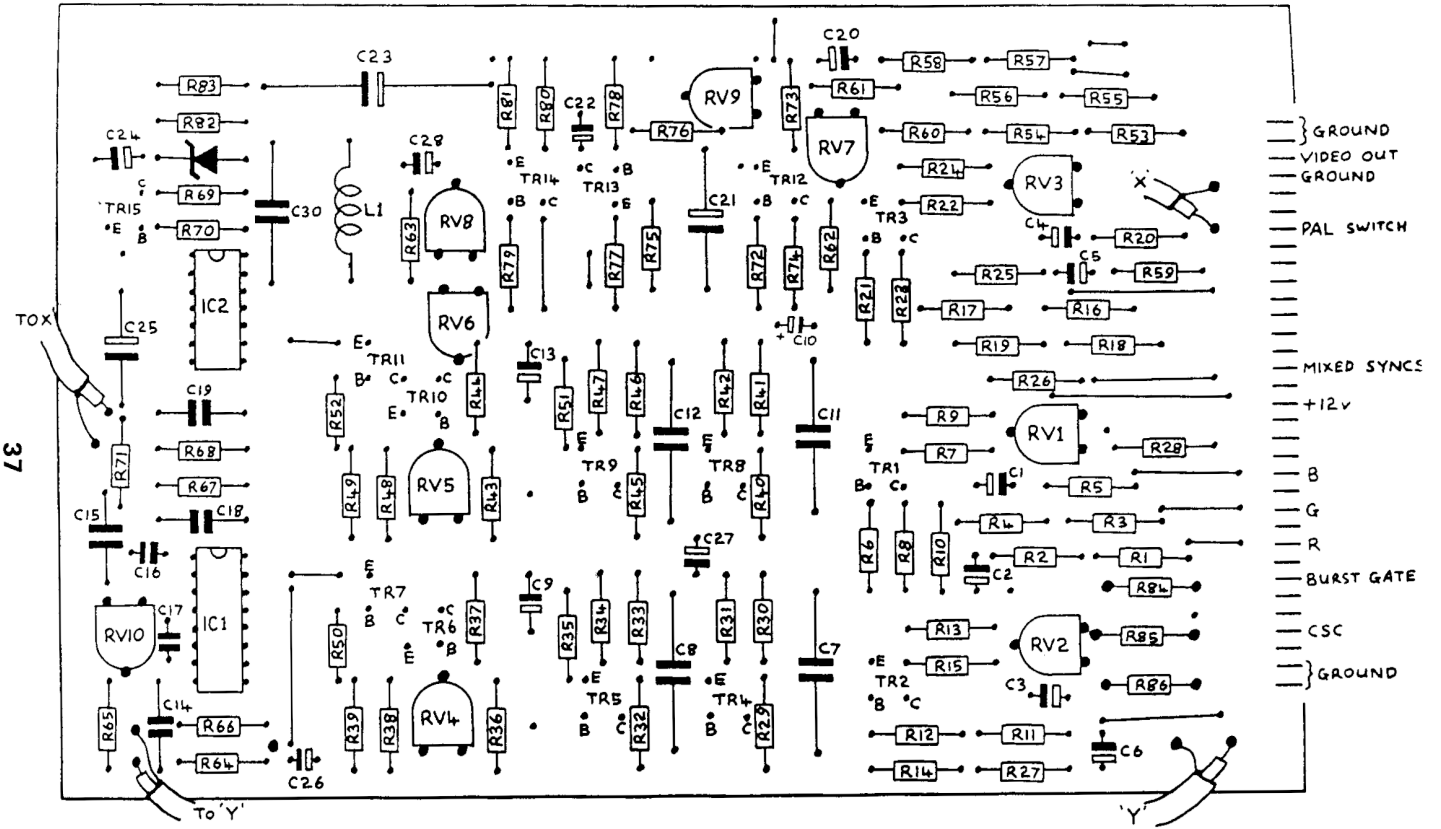
6. Burst phase.

BURST PHASE RV2 is difficult to adjust without a vector scope, however the setting is not critical and could be set to mid-position.

Scope. Adjust BURST PHASE RV2 so that the burst "pulse" in the R-Y chroma is the same amplitude (opposite polarity) as the burst "pulse" in the B-Y chroma signal.
Burst amplitude should then be 0.3v p-p - the same amplitude as syncs.

Mon/TV. Most domestic TVs will tolerate -50% to +200% variation in burst amplitude so the setting is not critical.
R26 in the R-Y matrix will alter burst amplitude and should this require changing in value to achieve correct operation then RV2 will require re-adjustment.

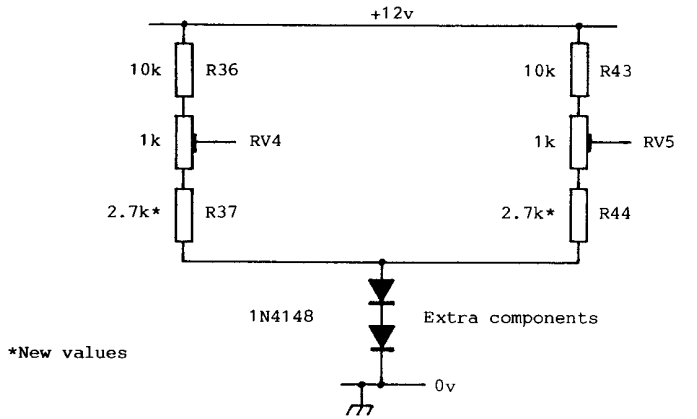
Whilst the input of the red, green and blue signals is matched to 75 ohms nominal which should prove to be sufficiently accurate, an exact match may be obtained by selecting resistors R84, R85 and R86 if desired.



COMPONENT LOCATIONS.

ADDENDUM.

Since this circuit first appeared in BATC Handbook-1, Brian Wade G8ABD devised a simple modification which was found to be beneficial in improving temperature stability. Modification involves lifting the earthy end of R37 and R44 and returning them to ground via 2 series 1N4148 diodes as indicated below. R37 and R44 should also have their values changed to 2K7. A further improvement in sub-carrier streaking after the test card red and white bars can be effected by increasing the value of C7 to 1uF.



CHAPTER 3
SECAM CODER

INTRODUCTION

by Jacques Pochet, F6BQP

The coder described below enables you to produce from the three primary signals red, green and blue together with synchronising pulses and a half-line rate switching signal, a composite SECAM colour signal. The details of this signal are as follows:

In colour television we distinguish two sorts of video signal, the luminance signal, called Y (which corresponds to a black and white signal), and the chrominance signals.
The luminance signal is defined by the fundamental colour weighting equation: Y = 0.299R + 0.587G + 0.114B.
The chrominance signals are the colour difference signals B-Y and R-Y.
The Y signal is transmitted as a classic black and white signal, while the B-Y and R-Y signals are in the form of a subcarrier modulated in frequency and situated at the top of the video spectrum towards 4.43 MHz. This is the basic principle which makes colour transmissions compatible with black and white ones.

Starting with these Y, R-Y and B-Y signals the receiver must retrieve the three primaries, R G and B. In the SECAM system the subcarrier is modulated alternately one line after the other by the B-Y and the -(R-Y) signal. The original or resting frequency of the subcarrier for the B-Y is FoB = 4250 kHz and for the -(R-Y) FoR = 4406 kHz.

To limit interference between the luminance and chrominance signals it is arranged that the instantaneous frequency of the subcarrier should not exceed 3900 and 4756 kHz. The maximum excursion thus for FoB is -350 to +506 and for FoR -506 to +350 kHz. Nominal excursion (for 75% saturated colours) is +-230 kHz for FoB and +-280 kHz for FoR. The chroma passband is limited to 1.4 MHz at -3dB (the Y signal retains all the necessary passband to transmit fine details of the picture).

Apart from this, the chroma signals undergo a preemphasis (the maximum of this is +8.5 dB at 750 kHz) to avoid high frequency components being lost in transmission noise. Before being incorporated in the luminance spectrum the subcarrier signal passes through an "anti-cloche" correction circuit, which is a notch filter centred on 4286 kHz and which has the effect of turning up the extreme side bands of the modulation. Inside the receiver the cloche (bell-shaped) curve restores proper amplitudes.

Finally, and this is only for older TV sets, nine identification lines are introduced into the vertical blanking interval, the frequency of the subcarrier during these lines being alternately 3900 and 4756 kHz. This allows the receiver to pinpoint the correct chroma senses. However, all TV sets made during the last three years function with line ident only and for these the frame ident is no longer necessary.

In professional coders the rest frequencies of the subcarriers are locked to the line frequency: FoB = 272 x fH and FoR = 282 x fH. The circuit shown

here uses a free running oscillator (multivibrator) but thanks to a certain number of precautions the stability obtained is sufficient for use under normal conditions. In order to trace chroma signals easily on an oscilloscope we use a normalised colour bar signal. The preemphasis provokes some ballistic shift, the amplitude of this being limited by clippers.

PRINCIPLE OF OPERATION OF THE CODER

The three signals RGB are added in a resistive mixer to form the luminance signal Y. The B signal is inverted by TR6 and added to the R and G signals to form the -(B-Y) signal. TR7 is an impedance matcher which leads to the low pass filter composed of 100uH and two 180 pF (matched to 500 ohm) which limits the chroma pass band. TR8 inverts the signal and achieves the preemphasis with its emitter decoupling. At the emitter of TR9 we have the B-Y signal at low impedance. This signal is clamped by TR10 to a fixed potential fixed by potentiometer
P5. It is this voltage which determines the rest frequency of the subcarrier oscillator.

The -(R-Y) is formed in the same way, with an additional phase inversion carried out by TR14.

The B-Y and -(R-Y) signals are then changed over on each line by a 4053 analogue switch and modulate the subcarrier oscillator made up of a multivibrator (TR23 and TR24). The chroma signal is then limited in amplitude by the clipper: TR20 prevents the signal from exceeding a threshold set by P8 and TR21 stops the signal from falling below a level set by P9. The two other 4053 analogue switches enable insertion in the vertical interval in the following manner: the combined sync pulses available at the collector of TR4 are integrated by the 100 Kohm and the 330 pF which allows the field syncs to be picked off, and after shaping by one of the 4066 analogue switches trigger two monostables in cascade (4528). The second monostable, with a period of 576 uS, defines the length of the nine ident lines inserted; during this time and thanks to the 4053 switch the chroma signal is replaced by two continuous voltage levels which make the clipper go high or low to give 4756 or 3900 kHz.

The subcarrier signal, frequency modulated, goes through a low pass filter to attenuate its harmonics, then undergoes the anti-cloche filter. It is amplified by TR5 and is passed to the output video amplifier. One gate of the 4066 analogue switch cuts off the subcarrier during sync pulses.

The treatment of the chroma takes a finite time and it is necessary to retard the Y signal to the same extent using a delay line. This should be in the order of 400 to 600 nS and could be found in an old junked TV set.

REMARKS

1. With the simplified type of video/sync mixer used here it is essential that the RGB signals are "clean", i.e. no signal during line and field blanking.

2. The base emitter junctions of TR19 and TR22 make up a temperature correction for any drift in the subcarrier frequency. This drift, after compensation, is in the order of -1 kHz per degree centigrade. Tests have shown that frequency errors start to cause visible changes of tints on the screen after frequency errors of +- 20 kHz. So if you make your adjustments at 25 degrees the coder should be usable at temperatures between +5 and +45 degrees C. The stability of the control voltages for the oscillator is assured by an 8 volt IC regulator, which is essential to guarantee good frequency stability.

3. The sync pulses together with the half line frequency switch are normalised at 2 volts into 75 ohm. TTL signals may be used direct if the 82 ohm terminating resistors are removed.

PRACTICAL CONSTRUCTION

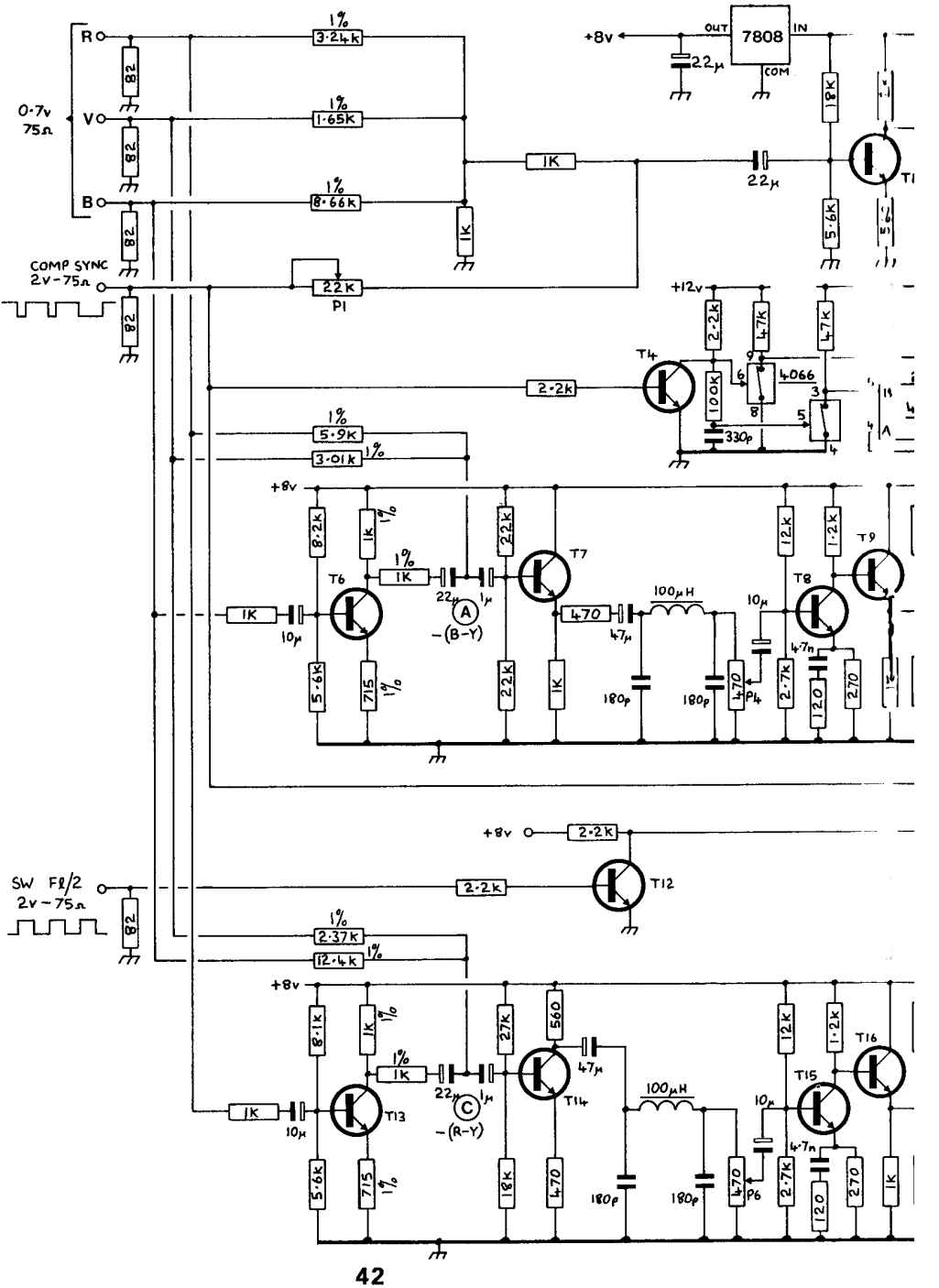
Construction is carried out using a double sided printed circuit board with the upper face used as a ground plane. The ground plane is removed around the holes of the components to avoid undesired shorts. Connections to ground are made direct to the upper face of the board without holes. Integrated circuits are placed in sockets.
The 3.9 and 100 uH inductances are non adjustable moulded coils (e.g. Orega). The coils in the anti-cloche circuit should be adjustable and can be made up as follows:
1.9 uH = 15 close turns of 0.3 mm enamelled wire on a 7 mm former with adjusting slug.
3.8 uH = 22 close turns of 0.2 mm enamelled wire on a 7 mm former with adjusting slug.

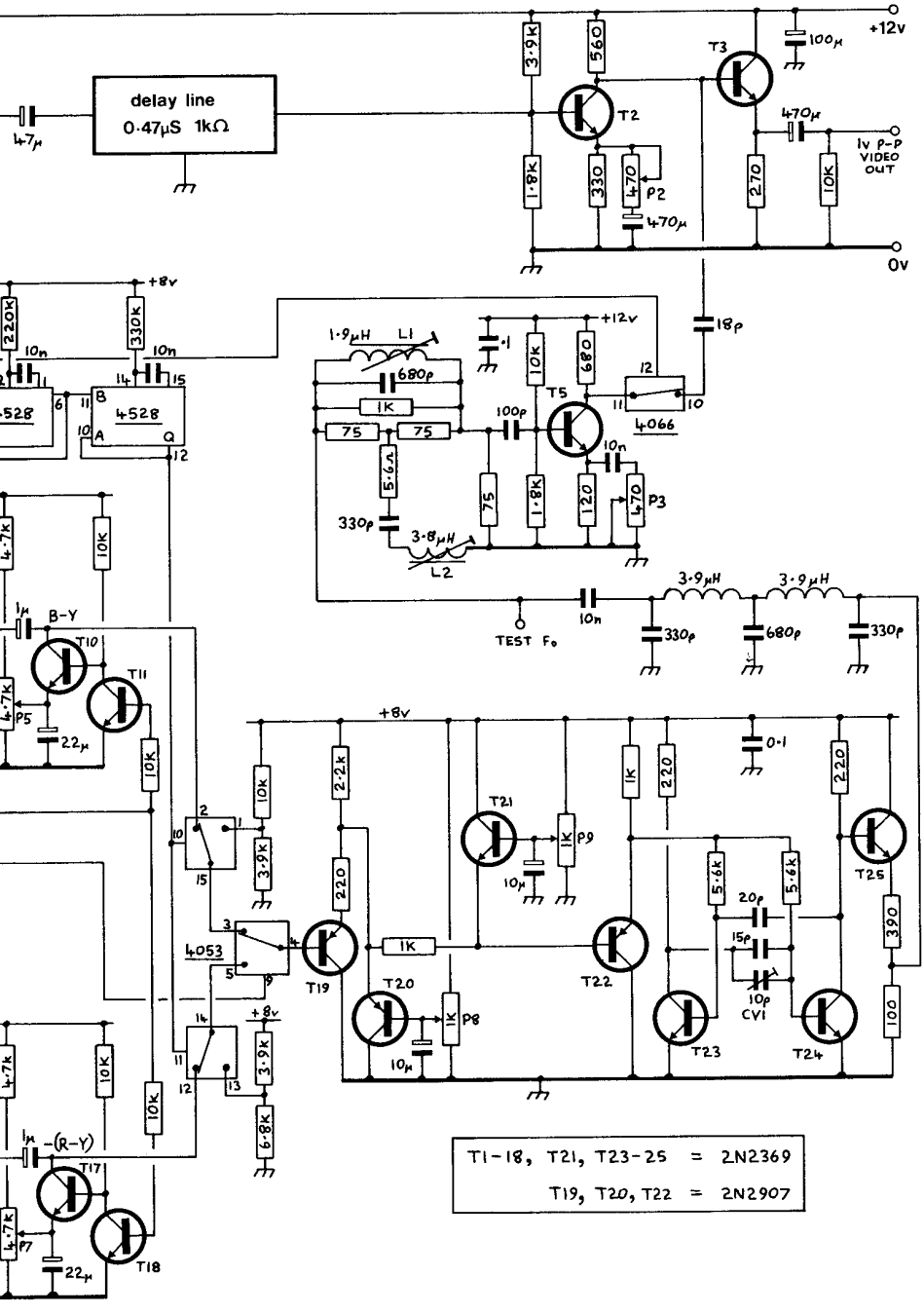
SETTING UP

1. Adjust video and sync levels.
Remove the 4066 from its socket (to suppress the subcarrier). Terminate the video output in 75 ohm and connect the scope there. Inject 0.7 Vpp (pp = peak to peak) signals into R G and B. Adjust P2 to have 0.7 Vpp of video amplitude at the output (not counting the sync pulses). Now adjust P1 to get 0.3 V of sync, so as to have a composite video signal of 1 Vpp amplitude.

2. Verify white balance.
Link RGB together and inject a low frequency signal (e.g. 10 kHz) of 0.7 Vpp amplitude (note that the terminating resistance is only 25 ohm here). Check with the scope that at points A and C that the amplitude of the signal is less than 10 mVpp. If not, adjust the emitter resistors of TR6 and TR13 to obtain minimum voltage. If you have used 1% resistors there should be no adjustments to make.

3. Set rest frequencies for FoB and FoR.
Connect a digital frequency counter to the point marked "Test Fo". Adjust F8 so that the rotor is at the +8 V end and P9 is at the earthy end (with the clipper out of service). Take out the 4053 from its socket and inject a continuous voltage at the base of TR19. Adjust CV1 to obtain the following voltage /frequency combinations*


R
V
B
0·7v
75Ω
COMP SYNC
2v-75Ω
SW F2/2
2v-75Ω
82
1%
3·24k
1·65K
8·66k
1K
22K
P1
2·2K
5·9K
3·01k
2·37K
12·4k
+8v
+12v
OUT
7808
IN
COM
22µ
18K
5·6K
T1
T4
2·2k
4·7K
100K
4066
330p
8·2k
T6
T7
22K
10µ
5·6K
715
470
47µ
100µH
180p
T8
T9
12K
1·2K
2·7K
4·7n
120
270
P4
T12
8·1k
T13
T14
27K
560
T15
T16
18K
P6
A
-(B-Y)
C
-(R-Y)



T1-18, T21, T23-25 = 2N2369

T19, T20, T22 = 2N2907

Voltage on TR19 base	Frequency
2.7 V	3900 kHz
3.25 V	4250 kHz
3.5 V	4406 kHz
4.0 V	4756 kHz

Replace the 4053 in its socket. Leave RGB in mid-air and connect sync pulses. Link pin 5 of the 4066 for the time being to ground in order to suppres the field ident lines (or remove the 4066 from its socket).
Tie SW to ground and ajust P5 to obtain 4250 kHz.
Tie SW to +2 V and adjust P7 to obtain 4756 kHz.

4. Setting clipping levels and field ident lines.
Remove the 4053 from its socket. Link pin 4 of the 4053's socket to pin 1, then adjust P9 to obtain 3900 kHz. After this, link pin 4 to pin 13 and adjust P8 to obtain 4756 kHz.

5. Adjustment of anti-cloche circuit and subcarrier level.
Having taken the 4053 out of its socket, connect a voltage to the base of TR19 so as to obtain 4286 kHz. Connect the oscilloscope to the base of TR5. Now adjust L1 and L2 for the smallest peak to peak voltage on the scope. This should be about 80 mVpp.
Still with 4286 kHz, adjust P3 to obtain 160 mVpp of subcarrier at the video output.

6. Setting the frequency excursions.
This adjustment should be carried out with the aid of a colour bar pattern which you inject as RGB. For 525 mVpp signals (75% bars) adjust P4 to obtain 700 mVpp at the emitter of TR9 and adjust P6 to obtain 850 mVpp at the emitter of TR16.

Note: when making peak to peak measurements of chroma signal amplitudes pay no attention to over voltages caused by the preemphasis.

BATC MEMBERS SERVICES:

Peter Delaney, G8KZG
6 East View Close,
Wargrave,
Berks. RG10 8BJ

CHAPTER 4

THE HOME COMPUTER

There is no doubt that the personal home computer is making great inroads into Amateur Television. Computer generated graphics can be seen on the airwaves, serial numbers and callsigns are displayed using computer generated graphics and contest points, distance between QRAs or QTHs are often calculated by means of a home computer as are beam headings. Even our club magazine CQ-TV is now computer processed.

In this chapter we shall be looking at how one of the most popular home computers, the Sinclair Spectrum, works, how to build specialist hardware and specific programs that make it suitable for Amateur Television applications. We will also be looking at amateur television programs for the BBC home computer.

If at the moment you do not own a home computer and are thinking of investing, the Sinclair Spectrum is an ideal starting point. Don't be put off by the admittedly inferior keyboard: many manufacturers make keyboards that are a direct plug in replacements which add that "up market" touch.

The Sinclair Spectrum also operates on 9 volts with internal inverters providing negative and +12 rails so it is ideal for portable operation. While on the subject of the inverter TR4 (ZTX651) is a little prone to failure, so check the -5 volts across C47 if you have any problems. Replacing TR4 with a BFY52 seems to fix any future recurrence.

Fig.1 shows the block diagram of the Spectrum. The CPU (central processing unit) is a Z80A which is an 8 bit CPU. This means there are 8 separate connections to its data bus. The CPU can send information to other devices in the Spectrum along this databus and other devices can send data back to the CPU along this same data bus. Because there are eight connections, each one of which can be either a logic 0 or a logic 1, any number between 0 (all zeros) and 255 (all ones) can be sent via the data bus.

Before the CPU can start doing anything it must be instructed what to do. The instructions for running BASIC are held in memory. The BASIC operating system is written in machine code and stored in the memory. The memory is made up both of RAM (random access memory) which is volatile (it forgets when power is removed) and ROM (read only memory), which does not forget when power is removed but can not be written into by the computer. The BASIC operating system is stored in the ROM part of the memory.

Once the program has told the computer what to do the CPU must get its inputs from the keyboard or cassette. The ULA helps the CPU interface with the outside world: the cassette interface circuits are in here along with the TV sync pulse generator and character generator. ULA stands for uncommited logic array and is a Ferranti chip containing a large number of unconnected logic gates. It can then be customised to form any circuit configuration required. In this case it is customised to a circuit designed by Sinclair and houses almost all the circuitry of the microcomputer with the exception of CPU and memory.

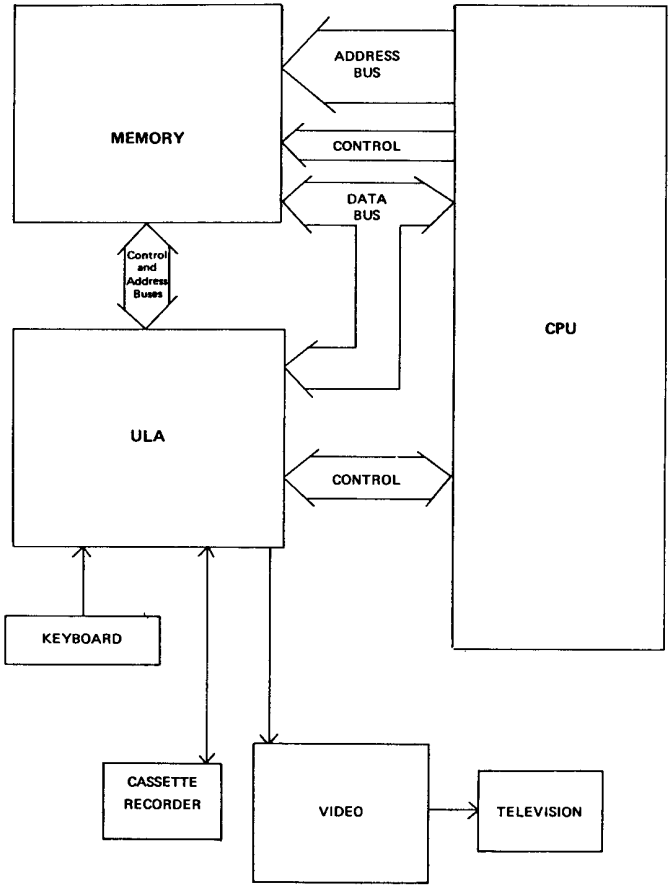


Fig.1 SPECTRUM BLOCK DIAGRAM

The keyboard is interrupt-driven which means 50 times per second the ULA interrupts the CPU so it stops doing whatever it is doing and lodges the current task in a part of memory known as the stack. It then services the keyboard scanning routine to see which push button has been pressed and responds accordingly. When the keyboard has been serviced the CPU returns to the stack, picks up its old job and resumes this until the next interrupt.

When data is being transferred by the CPU various control signals are generated: for example RD is generated when the CPU wishes to read data. WR is generated when the CPU wishes to write data into memory or IO (input/output).

An address is also generated by the CPU when executing memory read or write so as to indicate where in memory it wishes to read or write. The Z80A address bus has 16 bits, i.e. it can support 65,536 memory locations.

Both the memory buses and the data buses are digital meaning they can only carry ones and zeros, where logic zero is a condition between 0 and 0.8V and a logic 1 is a condition between 2 and 5 volts.

There is much specialist information available on the Z80A micro and in this limited space a drawing of the pin base and a description of pins other than address and data (which we have already covered) will have to suffice.

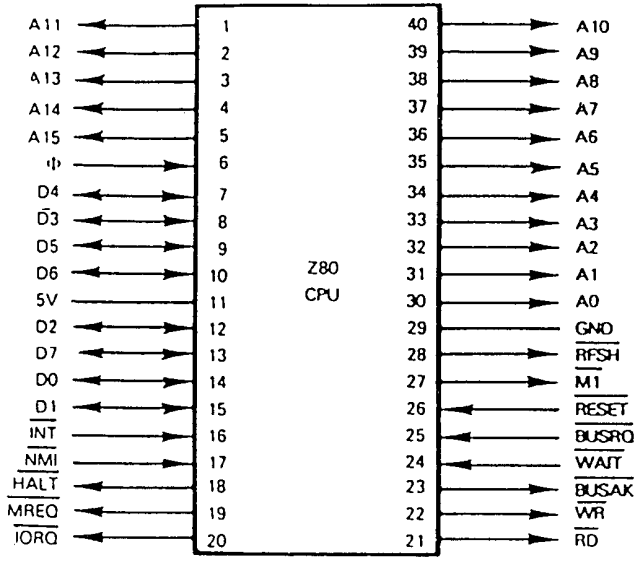
Pin 6 CLOCK input. On this pin we feed the Z80A with its clock - unlike some micros a complex clock is unnecessary and a simple crystal oscillator up to 3.5MHz will suffice. The only criteria are that its transitions must be fast and a 50/50 mark/space ratio must be maintained for high speed operation.

Pin 16 INT Interrupt request. This pin is active low and is an input to the Z80 to stop it executing its current task, lodge that task in stack and run a special machine code routine in memory. In the case of the Spectrum the keyboard is serviced in this way.

Pin 17 NMI Non maskable interrupt. Again this is an active low input to the Z80; when activated the micro will jump to memory location 102 (66HEX) and execute the programme there (re-initialise Basic in the case of the Spectrum).

Pin 18 HALT. This pin is an output of the Z80 and goes low when the CPU has executed a software halt.

Pin 19 MREQ. An active low output that signals that the address bus now contains a valid memory address which can be read or written to.



Pin 20 IORQ Input/Output Request. Active low and indicates that the address bus A0 to A7 holds a valid I/O address.

Pin 21 RD. Active low and indicates that the CPU wishes to read from memory or I/O.

Pin 22 WR. Active low and indicates that the CPU wishes to write to memory or I/O.

Pin 23 BUSACK. Active low and works with BUSREQ, pin 25, in that external devices requiring exclusive use of the data and address buses can request this by pulling pin 25 low. The micro signals back you have the bus by putting pin 23 low.

Pin 24 WAIT. Active low input to the CPU used by slow memory to tell the CPU they are not yet ready.

Pin 26 RESET. This input forces the CPU to reset state. In the Spectrum C27 holds the reset low until it has charged by R41. This allows the rest of the computer to reach an operational state before the CPU starts to run the program from address zero.

Pin 27 M1. Machine cycle 1. This output goes low to signal that the computer is currently getting the OP code for the next instruction to be executed from memory.

Pin 28 RFSH. Active low output which indicates that the address bus A0 to A7 contains refresh addresses for dynamic memories. All RAM memory can be divided into two types, static and dynamic. Static works by setting or clearing a flip flop depending whether we wish to store a logic 1 or a logic 0. Dynamic RAM works by charging or discharging a capacitor, but as capacitors will not hold a charge indefinitely then some system of replacing that charge must exist ie refresh. All 16k RAM is dynamic and the extension RAM is pseudo-static, i.e. dynamic with its own on-chip refresh.

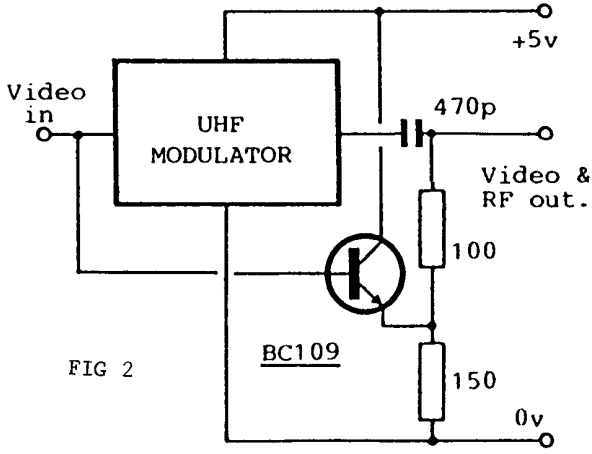


FIG 2

Having now digested a little on the theoretical side of our Spectrum let's move on to practical things.

The first use for a Spectrum in our TV station must be as a video generator and the first problem we encounter is that it has no video output, only RF suitable for connecting to a TV set.

Fig. 2 shows how to put all this right. The 20 pF capacitor can be fitted inside the modulator compartment by removing all the connections from the phono socket and fitting the 20 pF capacitor between them and the socket. Use a physically small capacitor so as to create minimum disturbance to the modulator layout. The 75 ohm resistor is also fitted to the phono socket inside the modulator compartment and routed to the outside world through

the spare hole at the connection end of the modulator can. Video input to the modulator is the centre connection on issue 3 Spectrums and +5V is available on the end connection. The transistor can be mounted outside the modulator case by soldering it directly to these connections along with the 330 ohm resistor, which earths to the can. This work will invalidate your

guarantee but by exercising a little care the process could be reversed and leave no traces behind if your Spectrum should need to be repaired under guarantee.

The phono socket now carries both RF at channel 38 and video which is suitable for driving a TV monitor directly. The two signals are far enough apart in frequency not to cause any mutual problems when sharing the same socket.

The video the Spectrum generates does leave a little to be desired in that its frame sync is a simple slab pulse devoid of any broad pulses and lacking proper interlace. The line waveform is fine, in fact better than the more expensive BBC computer in that the burst is positioned correctly on the back porch. The PAL coder is better (an LM1889, see Handbook 2) as opposed to a discrete TTL switching system in the BBC.

R*

22K @ 5v
33K @ 9v
47K @ 12v

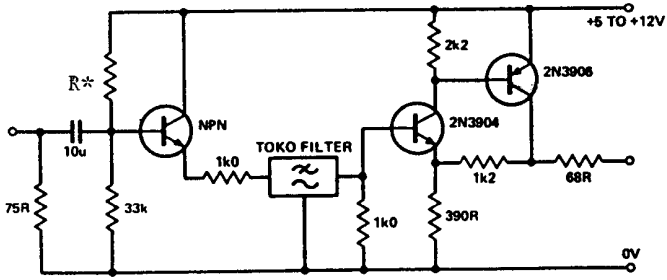


FIG 3

Before we let loose the video from our Spectrum or any other computer on the airwaves a good low pass video filter is recommended. Fig.3 shows the circuit of a good low pass video filter. It is based on the TOKO low pass linear phase video filter. The circuit will function on a variety of different voltage power supplies simply by changing the value of a resistor to set the operating point of our first transistor. The TOKO filter unit is available from Cirkit (formerly Ambit) and is a 23LVS1110 which has a bandwidth of 4.5 MHz at its 3 dB points. Where video bandwidth can be restricted further, in such times as contests and in areas of high television activity, the 23LVS1109 filter should be used. This filter has a bandwidth of 2.3MHz at its 3dB points. A printed circuit board is available for this project. Fig. 4 shows the component layout.

Now we have our computer generating video the next problem we come to is the size of the characters. The characters are quite readable on the shack monitor, but not all ATV contacts are made over a noise-free path. To increase the size of your characters simply type in program 1.

```
 10 RUN 9020
100 FOR Y=0 TO 179 STEP 36
110 FOR X=0 TO 255 STEP 32
120 PAUSE 0: BEEP .05,32
125 LET P=PEEK 23560
130 IF P=12 THEN RUN 100
140 GO SUB 8000: NEXT X: NEXT Y
150 INPUT LINE A$: RUN 100
8000 LET W=4: LET H=4
8810 POKE 23297,175-Y
8820 POKE 23298,W: POKE 23299,H
8830 LET C=15360+8*P: LET D=256
8840 POKE 23548,C-D*INT (C/D)
8845 POKE 23549,INT (C/D)
8850 POKE 23296,X
8860 LET L=USR 65000: RETURN
8865 DATA 42,141,92,34,143,92
8870 DATA 237,75,0,91,237,67,176
8880 DATA 92,237,67,254,91,6,8
8890 DATA 197,42,252,91,126,50
8900 DATA 129,92,35,34,252,91
8910 DATA 237,75,2,91,197,58,129
8920 DATA 92,6,8,197,203,23,237
8930 DATA 75,1,91,197,48,15,229
8940 DATA 213,245,237,75,176,92
8950 DATA 197,205,229,34,193,241
8960 DATA 209,225,237,75,176,92
8970 DATA 12,237,67,176,92,193
8980 DATA 16,226,193,16,216,237
8990 DATA 75,254,91,5,237,67,176
9000 DATA 92,237,67,254,91,193
9010 DATA 16,194,193,16,175,201
9020 CLEAR 64999: LET B=0
9030 FOR F=65000 TO 65101
9040 READ A: POKE F,A
9050 LET B=B+PEEK F
9060 NEXT F: BEEP .1,20
9080 IF B=13250 THEN GO TO 100
9090 PRINT "ERROR"
```

Program 1 GENERATE LARGE CHARACTERS.

```
1000 DATA 17,0,61,33,0,250,6
1010 DATA 96,197,6,4,26,119,35
1020 DATA 119,35,19,16,248,19
1030 DATA 19,19,19,193,16,238
1040 DATA 17,0,61,6,96,197,19
1050 DATA 19,19,19,6,4,26,119
1060 DATA 35,119,35,19,16,248
1070 DATA 193,16,238,201
1080 CLEAR 63949: LET Y=10
1090 FOR F=63950 TO 63999
1100 READ A: POKE F,A: NEXT F
1110 RANDOMIZE USR 63950
1120 DIM A$(45): INPUT LINE A$
1130 POKE 23607,249
1140 PRINT AT Y,0;A$( TO 32)
1150 POKE 23607,252
1160 PRINT AT Y+1,0;A$( TO 32)
1170 LET A$=A$(2 TO )+a$(1)
1180 IF CODE INKEY£=32 THEN GO TO 1200
1190 PAUSE 10: GO TO 1130
1200 POKE 23607,60
```

Program 3 DOUBLE HEIGHT, SCROLLING CHARACTERS.
(Merge with program 1)

If you type in an error in the data statement then 'Error' will be printed at the end. If all is OK a beep will be heard and then you are ready to type. The screen size is 8 characters wide by 5 lines deep. If you wish to use the machine code routine to use letters of a different size then adjust the variables X and Y for the X and Y co-ordinates on the screen. The variable W is width of the characters and H the height.

The delete function is used to clear the screen. If your computer is the BBC then the following program will give you a similar effect.

```
10 MODE 5
20 YS%=18:YS%=22
30 ON ERROR RUN
40 FOR Y%=1000 TO 200 STEP -200
50 FOR X%=100 TO 1220 STEP 160
60 A$=GET$:IF ASC(A$)<32 THEN 60
70 B=&C000+(ASCA$*8)-256
80 GOSUB 100:NEXT:NEXT
90 INPUT TAB(0,31)A:RUN
100 YY%=Y%:FOR G=0 TO 7
110 A=?B:XX%=X%:FOR F=0 TO 7
120 IF A/2<>INT(A/2) THEN GOSUB 150
130 A=INT(A/2):XX%=XX%-XS%:NEXT
140 B=B+1:YY%=YY%-YS%:NEXT:RETURN
150 PLOT 4,XX%,YY%:PLOT 1,XS%,0
160 PLOT 81,0,-YS%:PLOT 1,-XS%,0
170 PLOT 81,0,YS%:RETURN
```

Program 2

Program 3 enables your Spectrum to print double height characters which scroll across the screen in billboard fashion. The maximum length is 45 characters but this could be increased by changing the number in the DIM statement line 1120. The variable Y controls the position on the screen and can be any number from 0 to 20. To stop the routine simply press the space bar. If you accidentally break out of the program you may find the listing consists of strange looking characters. To get back to normal type GOTO 1200.

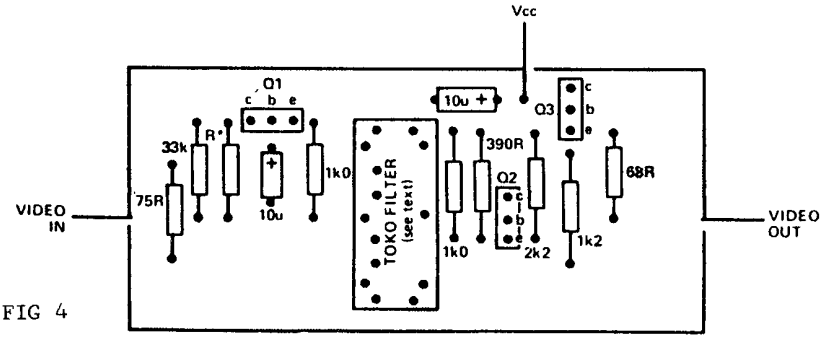


FIG 4

SPECTRUM USER PORT

PCB PROJECT

Having now mastered using the Spectrum as a video source we can turn our attention to using it in control applications. Fig.1 shows the rear edge connector of the Spectrum which carries the data, address, and control signals to and from the Z80 micro. Pin 17 is the $\overline{\text{IOREQ}}$; this pin is active low whenever the Spectrum is doing an input, output operation (input output request). This statement is not strictly true because Sinclair does use an $\overline{\text{IOREQ}}$ to do some functions within the computer. The A0 to A7 pins carry address information which means we can in theory access 255 I/O locations by decoding this part of the address bus. Sinclair use A0 to address the ULA, A1 Sinclair Printer, and A2 A3 A4 to control the Micro Drive, leaving A5 A6 A7 free for us to experiment with.

A7 along with $\overline{\text{IOREQ}}$ go low under the BASIC command IN 127 or OUT 127, depending whether we wish to receive or send data. $\overline{\text{RD}}$ will accompany the $\overline{\text{IORQ}}$ and A7 in going low on the BASIC command IN 127 and $\overline{\text{WR}}$ will accompany the $\overline{\text{IORQ}}$ and A7 in assuming a low under the BASIC command OUT 127. By use of TTL logic as per Fig.2 we can decode these commands and construct a simple user port.

When $\overline{\text{IOREQ}}$ A7 and $\overline{\text{WR}}$ are all low the 74LS175 quad latch is enabled. The D inputs are supplied with D0, D1, D2, D4 so whatever is on the lower part of the data bus when we enable the latch, i.e. IOREQ A7 and $\overline{\text{WR}}$ all going low will be latched and displayed on the LEDs and will also be available to the outside world as TTL commands on pins E, F, G, H, (Fig.2).

```
OUT 127,0 will turn all LEDs Off
OUT 127,1
OUT 127,2
OUT 127,4
OUT 127,8
```

will control each successive LED and the sum of the digits after the comma being used to switch more than one LED on at once, i.e. OUT 127,12 will switch the last two LEDs on simultaneously.

The next stage after getting the computer to issue commands to the outside world is to be able to send instructions to it. This we do by persuading the $\overline{\text{RD}}$ pin to go low under the instruction IN 127. This will enable the 74224 tri-state driver chip to connect inputs A B C D to the data bus and thus feed commands into our computer. The following short program will read and display the inputs A B C D on the screen.

```
10 PRINT IN 127
20 PAUSE 50
30 CLS
40 GOTO 10
```

The result should be 255 now: try grounding A B C and D in turn and the 255 will change i.e. grounding B should give 191. We can use this in BASIC by the following

```
5  PAUSE 10
10 IF IN 127 = 191 then GOTO 5
20 BEEP 4,4
30 GOTO 5
```

where a ground on pin B will put 191 on the data bus and keep the computer executing lines 5 and 10, removing the ground will cause line 20 to be executed and the Beep will result.

Let's try putting all this new found knowledge to use in ATV and design an ATV repeater. (Block diagram fig.5).

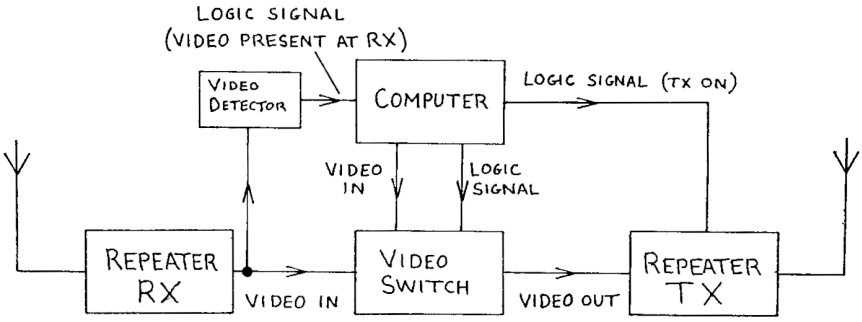


Fig. 5 TV REPEATER – BLOCK DIAGRAM

Fig.3 shows a circuit which will produce a logic 1 signal when fed with standard 625 line video signal. If this is fed into input B of our user Port then when video is present the data bus will display 255, and 191 when video is absent.

Fig.4 shows a logic-driven video switch which could be connected to E so OUT 127,8 would cause received video or computer video to be fed to the transmitter.

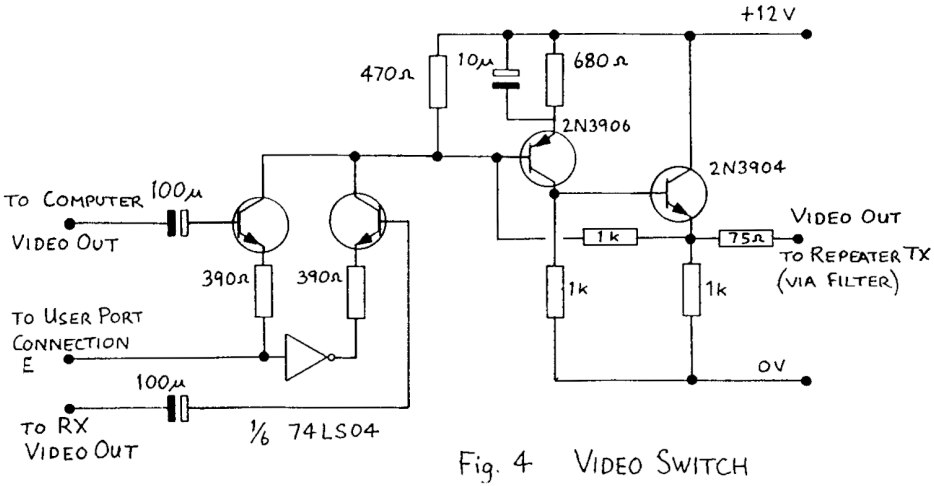


Fig. 4 VIDEO SWITCH

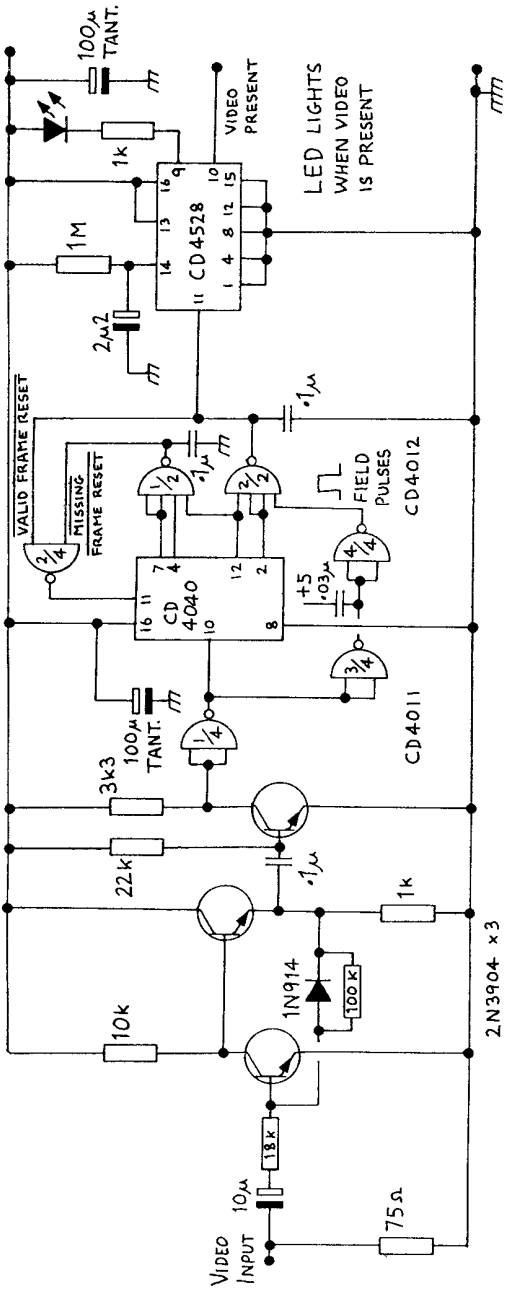


Fig. 3 VIDEO DETECTOR AND VERIFIER

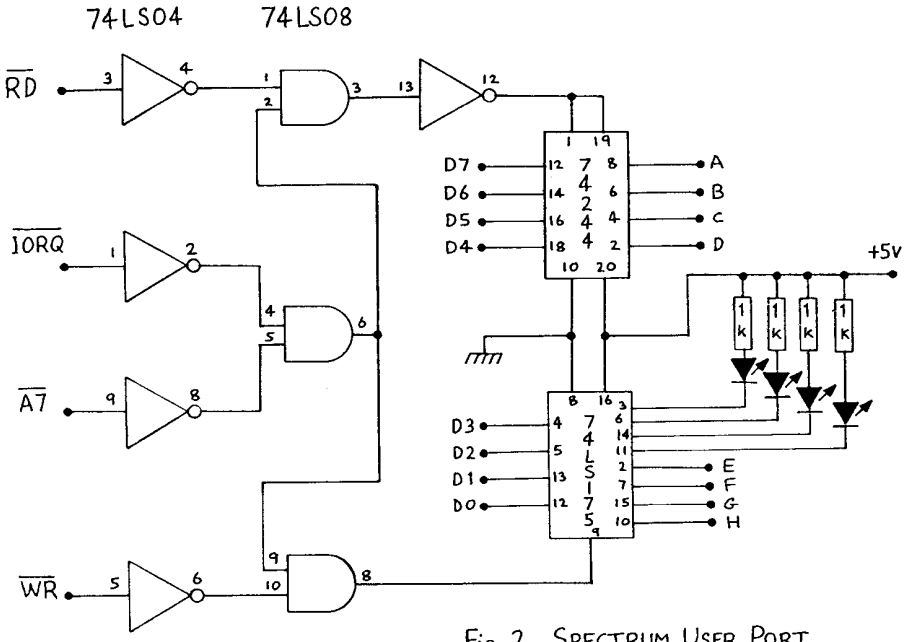


Fig. 2 SPECTRUM USER PORT

OUT 127,4 could control the transmitter on/off by using pin F to drive a relay which would switch on the transmitter. The following program could be used to drive an ATV repeater.

```
10 CLS : OUT 127,0: PAUSE 50
20 IF IN 127=191 THEN GO TO 10
30 PRINT "THIS IS GB8ATV"
40 OUT 127,4: PAUSE 200
50 LET X=20
60 IF IN 127=191 THEN GO TO 10
70 OUT 127,12: PAUSE 200
80 LET X=X-1
90 IF X=1 THEN GO SUB 500
100 GO TO 60
500 CLS :PRINT "TIME OUT"
510 OUT 127,4: PAUSE 200
520 OUT 127,0: PAUSE 20
530 IF IN 127=191 THEN RETURN
540 GO TO 520
```

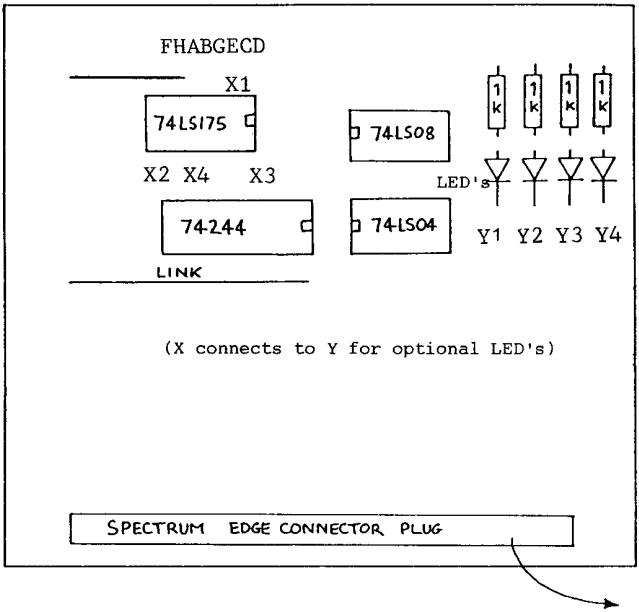
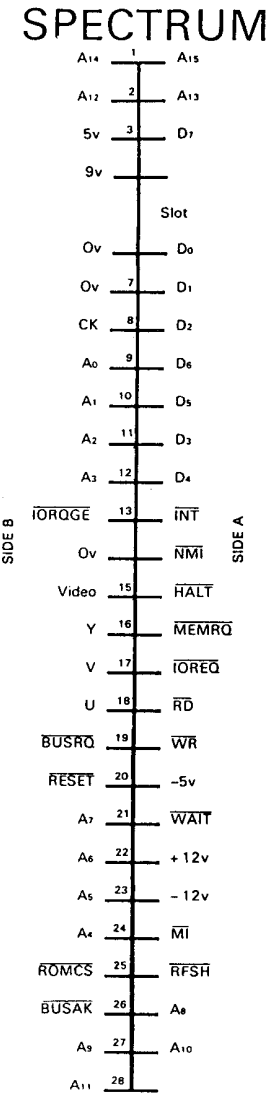


Fig. 6 SPECTRUM USER PORT P.C. LAYOUT



Viewed from front of plug.

COMPUTER CONTROLLING

CHARACTER GENERATORS

The original BATC character generator, which was based on a RO2513 ROM, first appeared in Handbook 1 and required a diode array to set up the characters. In Handbook 2 we added a piggyback memory board which gave keyboard access to the characters. The circuit in Fig.1 shows how to add an interface using only 1 chip which will allow the Spectrum to talk directly to the character generator and piggyback memory. The address used is A7, i.e. out 127, but this could be changed to A6, i.e. out 191. The character generator only requires a 6 bit code to select its characters, leaving data bits 6 and 7 spare. Data bit 7 is decoded in the 74LS138 to form a cursor home control. The decoded command appears from pin 14 of our decode chip and is inverted by TR1; it then goes to pin 14 of the 74193 on our piggyback board. The 150 ohm resistor which holds pin 14 down to ground requires removing. The BASIC command out 127,254 will set the cursor to the home position. The BASIC commands out 127,0 to out 127,64 will cause different characters to be printed: try experimenting by entering these commands in the immediate mode (i.e. no line number, just the command and then enter).

The following BASIC program will enable the character generator to be controlled by the computer keyboard. The characters produced will be upper case; the capshift does not require to be depressed so as to keep the operation as simple as possible. The enter key will home the cursor and bleep for acknowledgement of the command as the cursor is not displayed and so acceptance of this command is not obvious.

```
10 PAUSE 0
20 LET a$=INKEY$
30 LET b=CODE a$
40 IF b=0 THEN GOTO 10
50 IF b=13 THEN LET b=254 : BEEP .1,4: GOTO 70
60 IF b>96 THEN LET b=b-96
70 OUT 127,b
80 PAUSE 10
100 GOTO 10
```

Fig. 2 shows how we can extend this treatment to the new character generator which appears on page 7 of this book. Again a little extra hardware is required but in the case of this generator only a 74LS138, which can easily be mounted as in fig.2 on the keyboard module, by bending out the pins and fixing the chip in place with Superglue. The existing 74LS191 requires pins 1, 9, 10, and 15 joining together and pin 11 routing through to pin 14 of our additional chip (74LS138). Pin 15 of this new chip generates the strobe command which is routed through to the keyboard connector as is +5V and ground. The other pins of the keyboard connector go to the Spectrum data bus as shown. The 74LS138 is also connected to the Spectrum data bit 7, WR, A7 and IORQ.

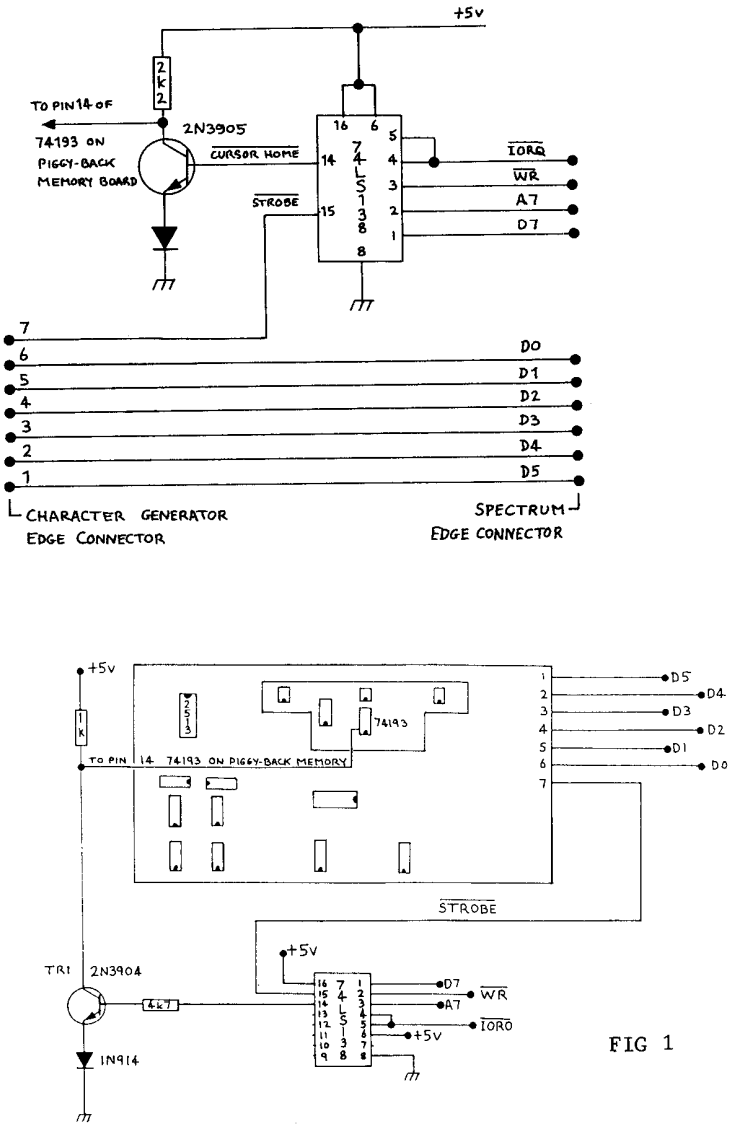

+5v
2K2
TO PIN 14 OF
74193 ON
PIGGY-BACK
MEMORY BOARD
2N3905
CURSOR HOME
STROBE
74LS138
IORQ
WR
A7
D7
7
6
5
4
3
2
1
D0
D1
D2
D3
D4
D5
CHARACTER GENERATOR
EDGE CONNECTOR
SPECTRUM
EDGE CONNECTOR
+5v
1K
2513
74193
TO PIN 14 74193 ON PIGGY-BACK MEMORY
D5
D4
D3
D2
D1
D0
STROBE
+5v
TR1
2N3904
4K7
D7
A7
WR
IORQ
+5v
1N914

FIG 1

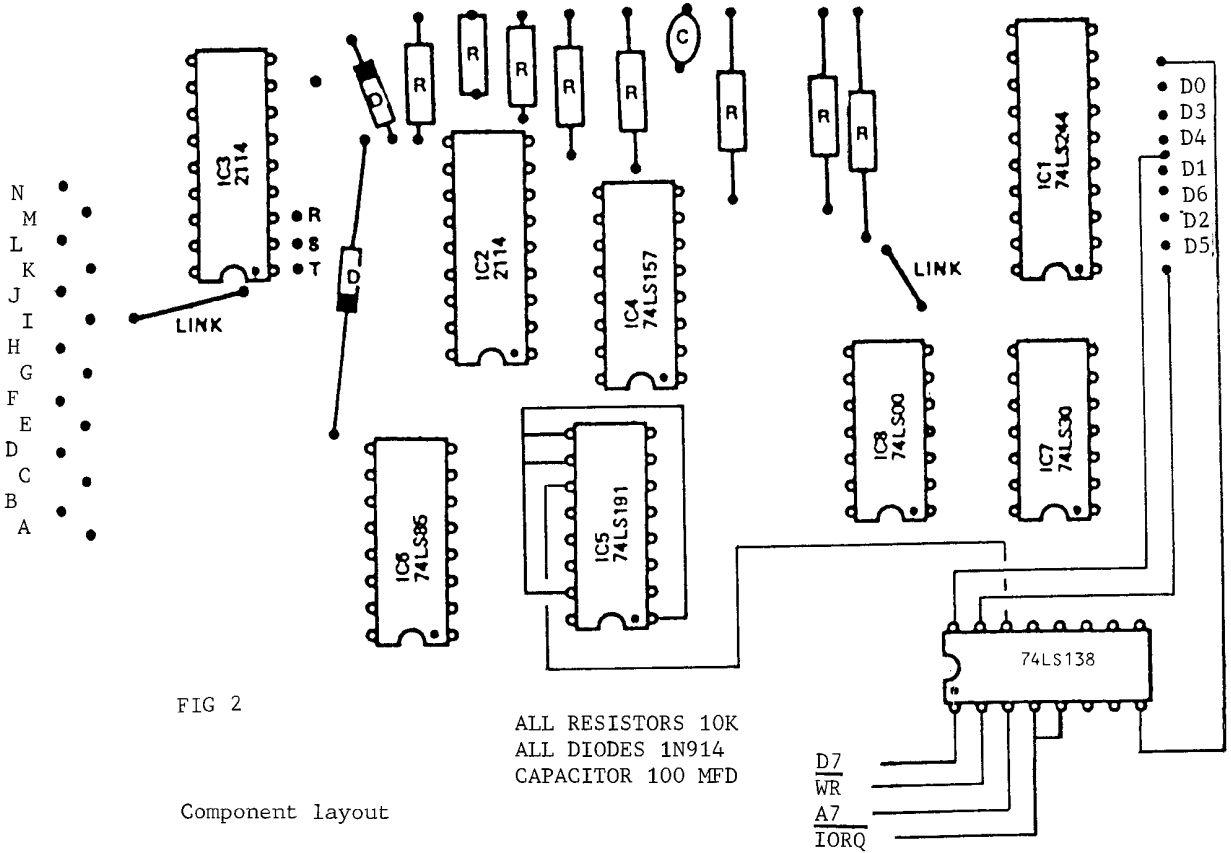


FIG 2

ALL RESISTORS 10K
ALL DIODES 1N914
CAPACITOR 100 MFD

Component layout

The keyboard program is a little different this time as the new character generator has lower and upper case characters along with some less useful teletext graphics (128 faces in all).

The enter key is a clear screen as well as a cursor home and the delete key performs the backspace function.

```
10 PAUSE 0
20 LET a$=INKEY$
30 LET b=CODE a$
40 IF b=0 THEN GOTO 10
50 IF b=13 THEN GOTO 1000
60 IF b=12 THEN OUT 127,127: GOTO 10
80 OUT 127,b
90 PAUSE 10
100 GOTO 10
1000 FOR a=1 TO 16
1010 OUT 127,32
1020 NEXT a
1030 OUT 127,254
1040 GOTO 10
```

These two programs show how once the computer is interfaced to the character generator it can double as a keyboard. But doubling as a keyboard is only one of its uses, it could be programed to animate your callsign around the character locations, or even keep time and display the hours, minutes or even seconds via the character generator. It's all down to your imagination and programming skills.

SPECTRUM PROGRAM TO PRODUCE THE BATC LOGO.

```
10 LET a=22528
15 FOR C=1 TO 104
20 READ b
25 POKE a+b,8
30 NEXT c
40 FOR d=22528 TO 23296
45 IF PEEK d<>8 THEN POKE d,48
50 NEXT d
55 BORDER 6
60 PAUSE 0
65 DATA 11,14,17,44,46,48,77,78,
79,105,106,107,108,109,110,111,
112,113,114,115,137,147,170,178,
203,209,236,240,268,272,300,304,
332,336,364,368,396,400,417,418,
419,423,424,428,432,436,437,438,
439,440,444,445,446,449,452,454,
457,460,464,470,475,481,482,483,
486,489,492,496,502,507,513,516,
518,519,520,521,524,528,534,539,
545,546,547,550,553,557,558,559,
566,572,573,574,590,619,620,621,
622,623,624,625,685,686,687,750
```

PCB PROJECT

SPECTRUM E-PROM PROGRAMMER

In the revised version of Amateur Television Handbook-2 a new character generator called "Soft Option" was introduced. One of the features of this new generator was that the character font was stored along with some pre-set graphics in Eprom. The text that accompanied the circuit explained how the data was arranged within the Eprom in order that you could create your own fonts and graphics.

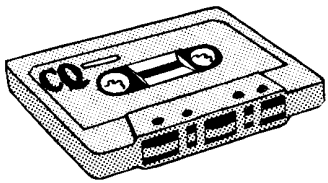
This circuit will provide the necessary hardware so that, when coupled to a Spectrum computer, you can programme your own Eproms. Besides the 2716 Eprom used in "Soft Option" this programmer will also programme the larger 2732 Eprom which is used in, for example, the SSTV Pattern Generator.

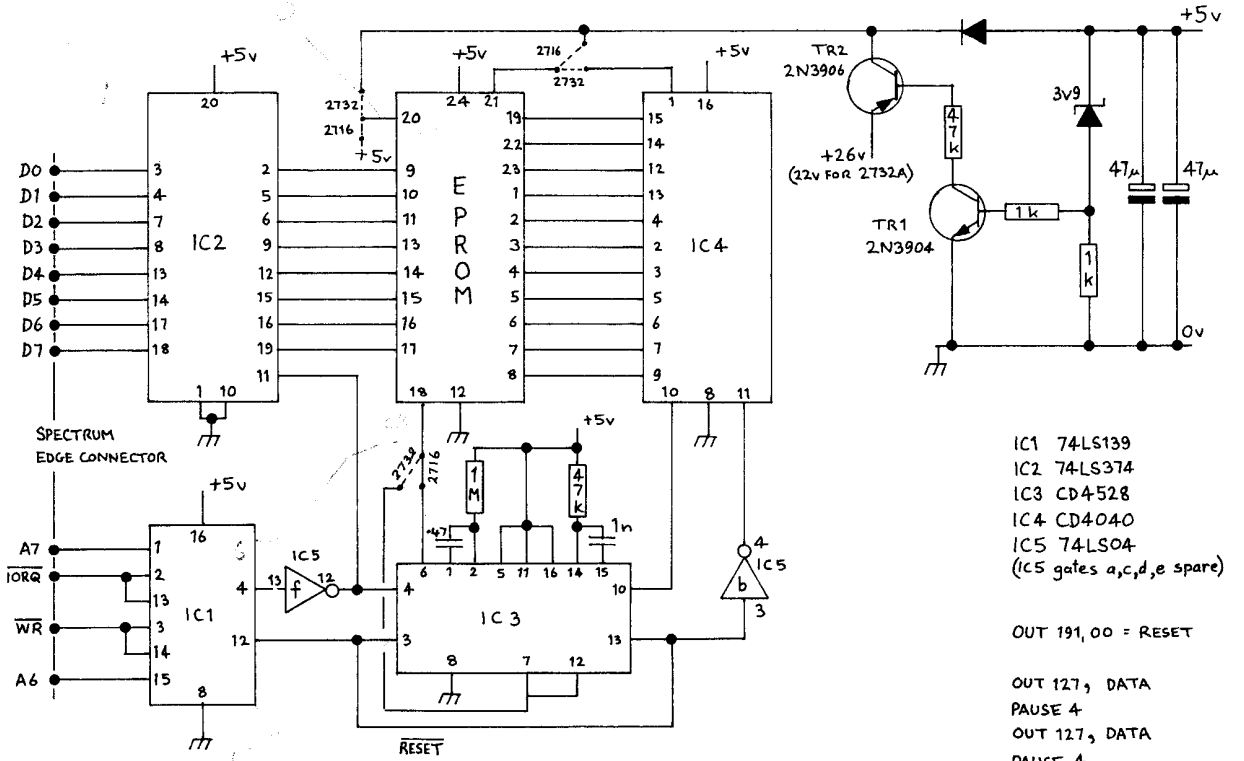
The programmer connects directly to the rear edge connector of the Spectrum using the data bus to receive the data word and the A6 and A7 lines along with $\overline{IORQ}$ and $\overline{W}$ to enable the programmer to decide which data is meant for it.

The first instruction it receives is OUT 191,00 which is decoded and used to reset IC4 (CD4040), a 12 bit counter. The next instruction OUT 127,data, signals that the first data word is present on the data bus. The word is latched in IC2 and presented to the data lines of the Eprom. IC3 (CD4528) is now triggered and a 50mS pulse is generated which programmes the Eprom. The programmer should not be presented with a new data word until this 50mS has expired. At the end of the pulse the 12 bit counter is advanced by one count, the counter is connected to the Eprom address bus and as such provides the address information to the Eprom. This means that, after the reset command, the first data word is stored at location 00 and the next at 01 and so on until all 2k of the Eprom is filled (or 4k in the case of the 2732).

The 2716 Eprom requires a +25v supply when it is being programmed, the 2732A requires only +22v. Only about 10 milliamps are drawn and a small battery could be used to provide this voltage. The circuit configuration varies slightly between the two types of Eprom and three links are provided which require setting to the appropriate position for each chip. TR1 and TR2 ensures that the programming voltage cannot be supplied without the +5v supply, as this would damage the Eprom.

Eprom programmers can only change a logic 1 to 0, so the first stage of programming is to expose the Eprom to ultra-violet light which changes all the data to logic 1's. This process is called 'washing'. Unfortunately, this simple programmer is unable to verify that the data has been stored correctly - the price you pay for simple circuitry!



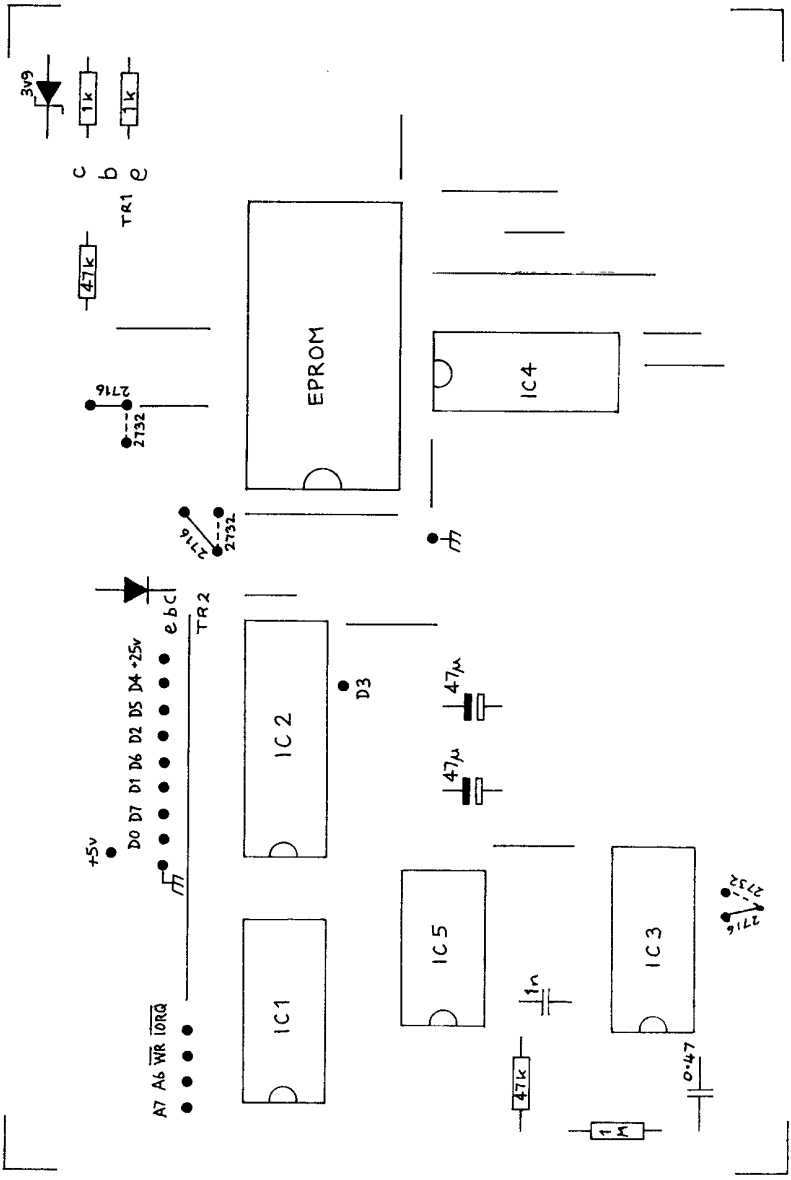


IC1 74-LS139
IC2 74-LS374
IC3 CD4528
IC4 CD4040
IC5 74-LS04
(IC5 gates a,c,d,e spare)

OUT 191, 00 = RESET

OUT 127, DATA
PAUSE 4
OUT 127, DATA
PAUSE 4
ETC.

SPECTRUM EPROM PROGRAMMER



PRINTED CIRCUIT BOARD COMPONENT LAYOUT

The simplest way to use this Eprom programmer is as follows :-

```
10 REM EPROM PROGRAMMER
20 OUT 191,00
30 FOR A=1 TO Z
40 READ D
50 OUT 127,D
60 PAUSE 4
70 NEXT A
80 PRINT "DONE"
90 DATA
```

Where the data words to be programmed are expressed in decimal and inserted in address order in data statements from 90 onwards. Z in line 30 is replaced by the total number of digits in the data statements.

If you are designing a PROM for "Soft Option", the character generator which appeared in the 'Revised Amateur Television Handbook', then the following programme will enable you to customise an Eprom and blow it all with the aid of a 64k Spectrum.

Enter the programme as shown carefully and save it to tape with the command SAVE "Eprom blow" LINE 0. When you run the programme you will be asked to enter a character between 1 and 256, that being the character you wish to define or re-define. You are now able to move the hash cursor around the grid with the cursor keys 5,6,7 & 8. If you want to ink-in part of the grid press ENTER and if you want to delete an ink spot then press zero. There are a few more commands which are obtained by using keys 1,2,3,4,9 and symbol shift & A:

Key 1. You are asked to enter a character 1 to 256 this enables you to define or re-define a character.

Key 2. On pressing this key you will be asked if you wish to blow the Eprom. If you are ready, press Y and press ENTER, whereupon the Eprom will be blown. If not, press N and then ENTER or just ENTER which will return you to the grid.

Key 3. You can save the data created by the defining of characters you have designed. If you do not want to save them just press ENTER and you will return to the grid.

Key 4. This will enable you to load back in the data previously saved. Again you can return to the grid by pressing ENTER.

Key 9. With this command you can quickly delete a whole character, pressing ENTER will return you to the grid.

Key symbol shift and A. This will restart the programme.

```
 10 REM By R.Stephens G8XEU
 20 CLEAR 59999: LET SET=256
 30 POKE 23658,8: GO SUB 900
 40 INPUT "ENTER CHARACTER 1 TO ";(SET);" ";CH
 50 IF CH<1 OR CH>SET THEN GO TO 40
 60 LET MEM=60000+((CH-1)*16)
 70 GO SUB 900: GO SUB 800
 80 LET X=5: LET Y=3
 90 BEEP .2,30: PRINT AT 21,5;"CHARACTER ";CH
100 PRINT PAPER 9; INK 8;AT Y,X;"#"
110 PAUSE 0: LET A$=INKEY$
120 BEEP .05,20
130 PRINT PAPER 9; INK 8;AT Y,X;"+"
140 IF A$="5" THEN LET X=X-(X>5)
150 IF A$="6" THEN LET Y=Y+(Y<18)
160 IF A$="7" THEN LET Y=Y-(Y>3)
170 IF A$="8" THEN LET X=X+(X<12)
180 IF A$=CHR$ 48 THEN PRINT AT Y,X;"#": GO SUB 300: GO TO 110
190 IF A$=CHR$ 226 THEN RUN
200 IF A$="1" THEN GO TO 40
210 IF A$="2" THEN GO TO 500
220 IF A$="3" THEN GO TO 700
230 IF A$="4" THEN GO TO 750
240 IF A$="9" THEN GO TO 600
250 IF A$=CHR$ 13 THEN GO TO 270
260 GO TO 100
270 PRINT PAPER 0; INK 6;AT Y,X;"#"
280 GO SUB 300
290 GO TO 110
300 LET C=0
310 LET D=1
320 FOR F=12 TO 5 STEP -1
330 IF ATTR (Y,F)<>56 THEN LET C=C+D
340 LET D=D*2
350 NEXT F
360 LET E=INT (C/16)
370 LET G=C-(E*16)
380 PRINT AT Y,20;CHR$ (G+48+7*(G>9));CHR$ (E+48+7*(E>9))
390 POKE MEM+(Y-3),(G*16)+E
400 RETURN
500 INPUT "DO YOU WISH TO BLOW THE''''EPROM Y/N "; LINE A$
510 IF A$<>"Y" THEN GO TO 90
520 PRINT AT 21,0;"E PROM BEING BLOWN PLEASE WAIT."
530 OUT 191,0
540 FOR F=MEM TO MEM+(SET*16)
550 OUT 127,PEEK F: PAUSE 4
560 IF INKEY$<>"" THEN GO TO 560
570 NEXT F
580 PRINT AT 21,8;"EPROM BLOWN"
590 STOP
600 INPUT "DO YOU WISH TO DELETE THIS''''CHARACTER Y/N "; LINE A$

610 IF A$<>"Y" THEN GO TO 90
620 FOR F=MEM TO MEM+15
630 POKE F,0: NEXT F
```

```
 640 GO SUB 900: GO TO 90
 700 INPUT "DO YOU WISH TO SAVE DATA Y/N"'; LINE A$
 710 IF A$<>"Y" THEN GO TO 90
 720 SAVE "DATA"CODE 60000,SET*16
 730 GO TO 90
 750 INPUT "DO YOU WISH TO LOAD DATA Y/N"'; LINE A$
 760 IF A$<>"Y" THEN GO TO 90
 770 LOAD ""CODE 60000: GO TO 90
 800 LET Y=3
 810 FOR J=MEM TO MEM+15
 820 LET POS=PEEK J
 830 IF POS=0 THEN GO TO 880
 840 FOR H=8 TO 1 STEP -1
 850 IF INT (POS/2)<>POS/2 THEN PRINT PAPER 0; INK 6;AT Y,H+8*(H
<5);"+"
 860 LET POS=INT (POS/2)
 870 NEXT H: GO SUB 300
 880 LET Y=Y+1
 890 NEXT J: RETURN
 900 CLS : PRINT AT 0,5;"CHARACTER DESIGNER"
 910 FOR F=3 TO 18
 920 PRINT AT F,5;"++++++++";TAB 20;"00"
 930 NEXT F: RETURN
```

RS232 E-PROM PROGRAMER

Cataloguing all the available PROM blowers on offer showed that there is a lack of one that will run on all machines. It was an article by G.Sullivan of Worcester that stimulated the following design.

The requirements were

1) standard connection to any computer - this is achieved by using the RS232 port;
2) simple programming, done by outputting a memory location to the printer port;
3) simple reading, done by the hardware sending back 'full duplex', i.e. the programmer sends back the EPROM contents after programming (a read after write). This simplifies the reading-verify and handshaking into minimal software.

In BASIC, it can be:

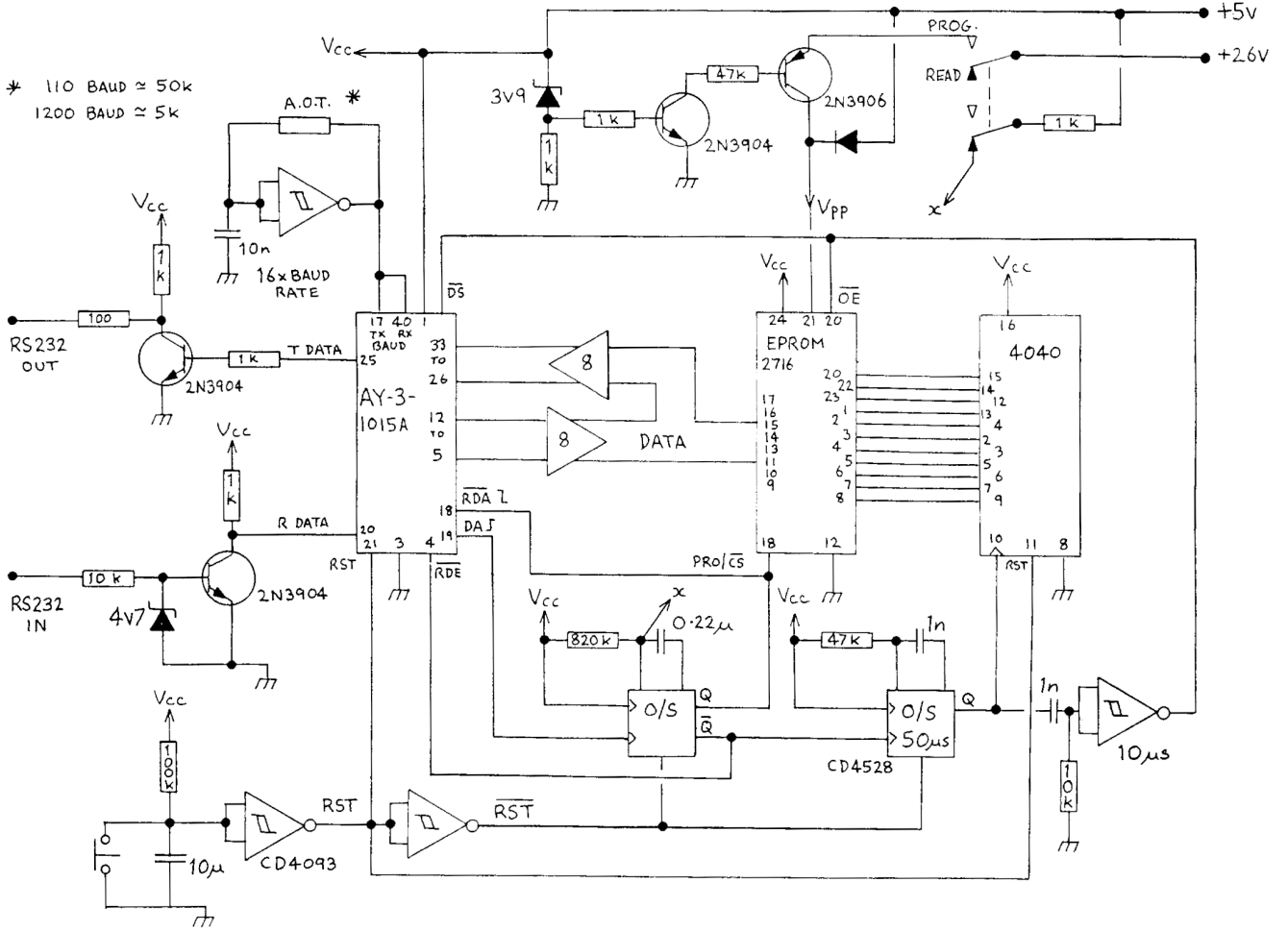
```
MEMORY = nnnn
For W = nnnn to nnnn + (EPROM size)
PEEK X, MEMORY
OUT(PRINTER PORT),X
Y = INP (PRINTER PORT)
IF X <> Y THEN PRINT "ERROR";W,X,Y
NEXT W
PRINT "OK - FINISHED"
```

THEORY OF OPERATION

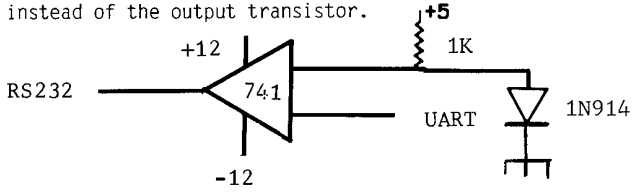
The 8 bit word is received by the UART which raises Data Available (DA) causing the 50 mS one-shot to apply the PROG signal to the EPROM. The address is supplied by the CD4040 which will be incremented by the end of the 50 mS pulse and the data supplied by the UART, when RDE is lowered by the 50 mS pulse. The 50 mS pulse also supplies RDA to reset DA for the next 8 bits to arrive. That process carries on until no more data arrives.

Because there is a 50 mS time penalty we can not send at more than 150 bits per second, but by using the handshaking any bit rate can be used, to a maximum of approximately 20 words per second. The handshaking is achieved by generating a 10 microsecond OE signal after the PRQ signal falls and becomes CS. The 10 microsecond pulse is also given to the UART at DS (data strobe) to take in the data bits from the EPROM and retransmit them back to the host.

If 26V is applied to an EPROM without the 5V then it dies, so a simple protection circuit using a 3V9 zener and two transistors cuts down the fatalities. If all we want to do is read an EPROM, then no 26V is applied

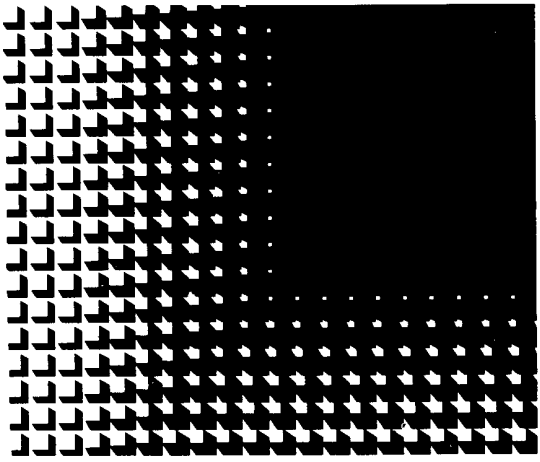

* 110 BAUD ≃ 50k
1200 BAUD ≃ 5k
A.O.T. *
Vcc
3v9
1k
47k
2N3906
2N3904
PROG.
READ
+5v
+26v
VPP
10n
16xBAUD RATE
DS
100
RS232 OUT
T DATA
AY-3-1015A
17 40 1
TX RX BAUD
33 TO 26
12 TO 5
8
DATA
EPROM 2716
24 21 20
OE
4040
16
R DATA
RS232 IN
10k
4v7
RDA
DA
RDE
RST
PRO/CS
820k
0·22µ
x
O/S
Q
Q̄
47k
1n
CD4528
50µs
10µs
100k
10µ
CD4093
RST
10k

and the 50 mS pulse is reduced so that you can read it at full bit rate speed. Programming still needs 50ms times eprom size, ie. 50 times 4K(2732) = 3 min. 20sec.. Because no negative supply is used the RS232 output is not correct but most micros don't need it; if yours does, then a 741 op-amp can be fitted instead of the output transistor.



We also require a reset push-button to be pushed before each read or write sequence and a baud rate generator that runs at 16 times the bit rate. The resistor values are only approximate because the capacitor and the CMOS invertor have unpredictable tolerances.

Finally, note that the CD4040 can address a 2732 but a few minor changes in the logic will be necessary as detailed in the E-PROM programmer for the Spectrum, elsewhere in this book. 2764, 27128 and 27256 E-PROMS, which have more pins, would need another holder and an extended addressing capability - say by toggle switch - to program as if they were blocks of 2732's. Texas 2532 chips are not catered for because of their non-standard pin arrangement, and remember that the newer faster E-PROM's have lower programming voltages, for example6 22v instead of 26v in the case of the 2732A. These programming voltages should be within +/- 0.25v for reliable programming and current is usually in the region of 10 to 20mA.

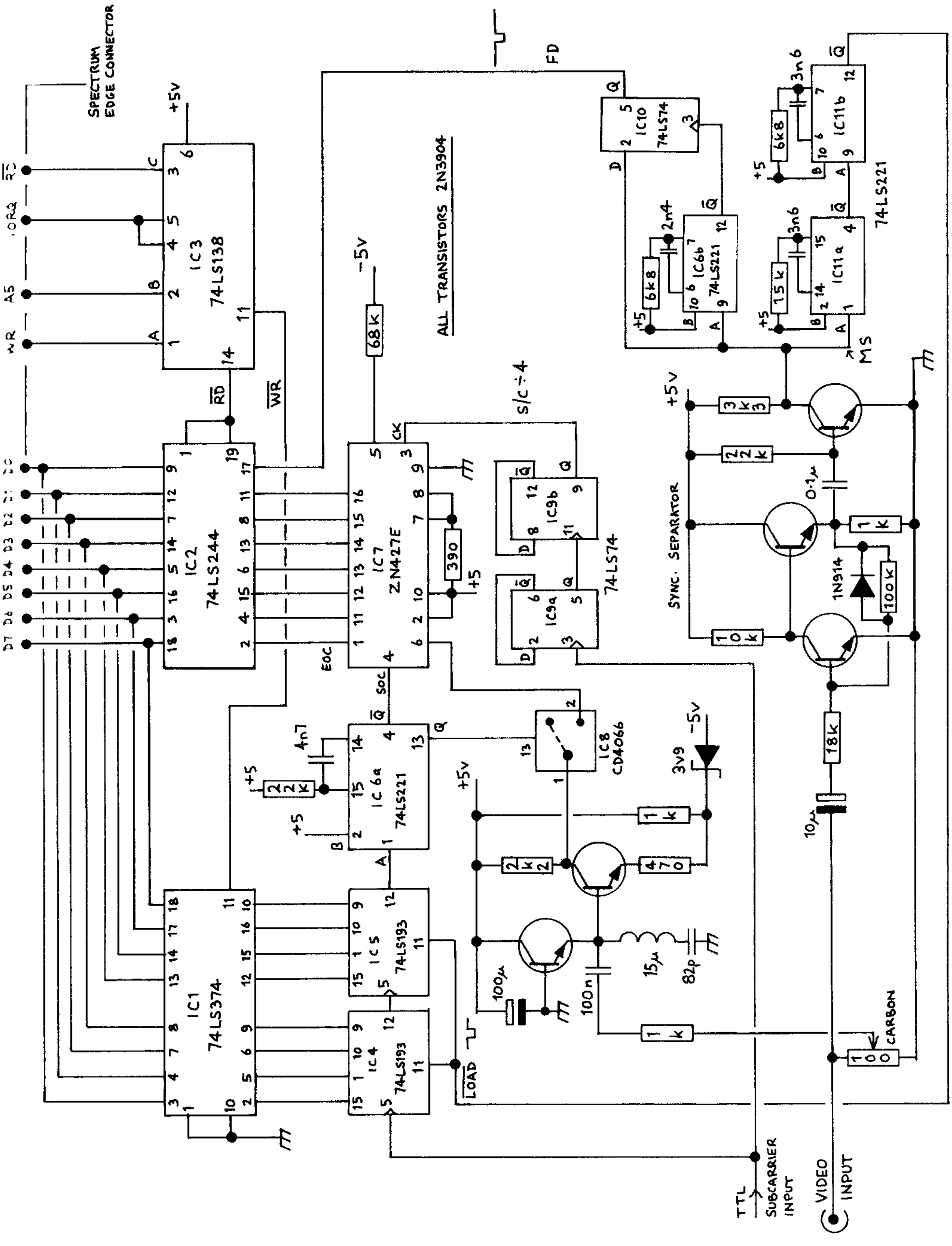


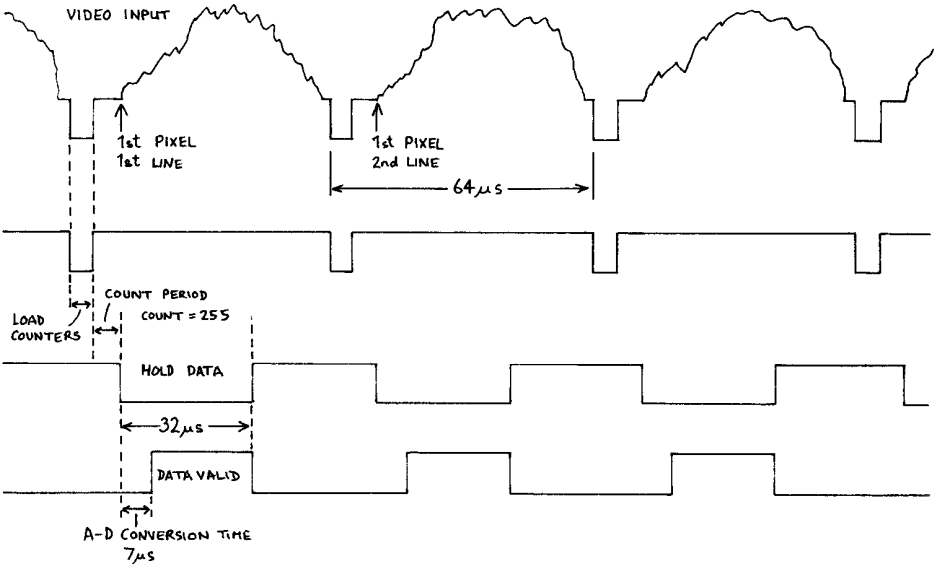
SPECTRUM FREEZER

One of the most obvious uses for a Home Computer is to take an incoming picture and freeze it in the computer's memory, so that it can be saved on to tape and re-used at a later date as part of a transmission. The way we do this is to convert the television picture into digital words that can be processed by the computer in the normal way. The first process in converting the picture into computer data is called Quantisation. In this process a television picture is broken down into pre-set brightness levels. The ZN427E IC, which accomplishes this task, is capable of 64 levels of grey. To store each individual pixel of a television picture, using a 6 bit word to represent a picture element, would consume a lot of computer memory, so some economies must be made. The first is to reduce the picture to only 16 brightness levels (a 4 bit computer word) i.e. 2 pixels can be stored in each byte of computer memory. Assuming 255 pixels for each TV line and 255 lines in a TV picture (average resolution), then this would require a little over 32k bytes of memory. This is well within the capability of a 64k Spectrum with its 48k of available user memory. For 16k Spectrum users, a solution may be to process 32 points on 24 lines, a total of 768 readings which could be displayed directly as character squares on a Spectrum screen, using attributes to give 8 shades of grey.

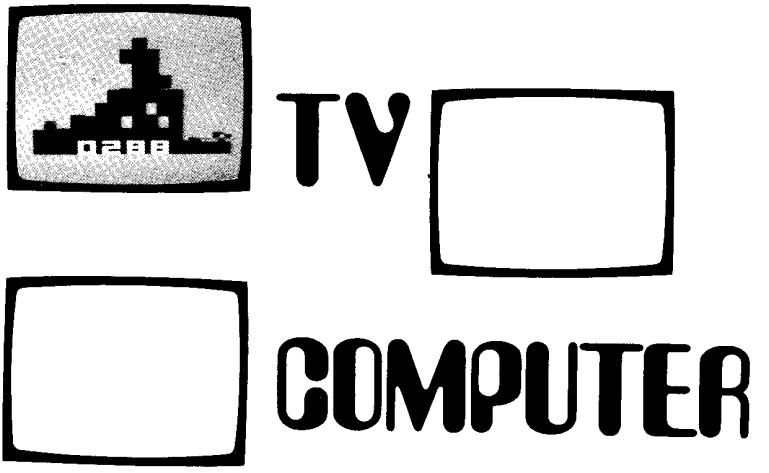
Fig.2 shows the circuit diagram of the necessary hardware in order to convert the television picture into the computer data. The first problem to be overcome is one of speed, given that the ZN427E will take up to 7uS to convert the first pixel of line 1 to a data word. The computer will also take time to store this data word in memory, so by the time the second pixel occurs it will not be able to process it. The way round this problem is to process the first pixel on line 1 and then the first pixel on line 2 and so on down the left hand edge of the television picture in a straight column, followed by pixel 2 on line 1, followed by line 2 etc. This gives 64uS between successive storage operations; sufficient time for the ZN427E and the computer to accomplish the task. The only problem is that the picture must be stationary for a few seconds whilst it is being stored.

The composite video signal is fed to a conventional sync separator and also to a small video amplifier to ensure that the ZN427E is correctly driven. Line sync pulses are used to load an 8 bit resettable counter. The preset number sent to this counter, by the computer, decides where along the line the picture is sampled. When line sync occurs, this number is loaded into the counter which is then clocked by a subcarrier clock until a count of 255 is reached. A carry pulse is then generated, which triggers the monostable for 32 micro seconds. During this time the video signal presented to the ZN427E is frozen in a sample and hold circuit, for the 7uS necessary for the conversion. The monostable also instructs the ZN427E to start converting. The end of digital conversion is signalled by the EOC pin, which signals the computer to read the picture data into memory. The ZN427E now reverts to reading-in the video signal. It is important that the EOC is switched off after 32uS because the software will soon look at the pin again and must latch to it and wait for it to go high. The separated field sync is also read by the computer each time it loads a digital word. This enables it to detect frame pulses, and to locate the top of picture.


SPECTRUM EDGE CONNECTOR
RD
IORQ
A5
WR
D0 D1 D2 D3 D4 D5 D6 D7
+5v
IC3
74LS138
IC2
74LS244
IC1
74LS374
FD
ALL TRANSISTORS 2N3904
-5v
68k
IC7
ZN427E
390
+5
EOC
SOC
S/C ÷ 4
IC9b
IC9a
74LS74
IC10
74LS74
IC6b
74LS221
IC11a
IC11b
74LS221
6k8
2n4
15k
3n6
MS
SYNC. SEPARATOR
3k3
2k2
0·1μ
1k
1N914
100k
10k
18k
10μ
IC6a
74LS221
4n7
2k2
IC8
CD4066
3v9
470
100μ
100n
15μ
82p
IC5
74LS193
IC4
74LS193
LOAD
CARBON
100
TTL
SUBCARRIER INPUT
VIDEO INPUT



SPECTRUM FREEZER TIMING DIAGRAM



The next problem, after storing the picture in computer memory, is that of displaying it. The screen of the Spectrum is 255 pixels by 175 which seems excellent resolution except when you realise that they can only be white or black. How then can shades of grey be displayed? The answer can be found by examining a newspaper picture, which is made up of clusters of dots. Each dot is the same shade, but more of them are clustered together for darker shades of grey. The grey scale is reduced further, to say, four shades of grey and this cluster of four pixels is used to represent dark grey, reducing the cluster by one as the shade gets lighter. The resolution is only 128 by 87 but still a recognisable picture. The alternative is to stay at 255 by 175 and have a digital-looking picture with no grey scale. The software allows this choice of display mode, which depends on picture content.

```
10 CLEAR 28415
20 LET a=28671
30 LET a=a+1
40 READ d:POKE a,d
50 IF d>0 THEN GO TO 30
60 PRINT "START TAPE"
70 PAUSE 0
80 SAVE "FREEZER" CODE 28672,245
90 STOP
100 DATA 33,0,0,175,50,8,92,1,191
,225,62,7,237,121,1,191,225,62,12
7,237,121,33,245,112,30,63,243,1,
191,255,62,14,237,121,1,191,255,6
2,255,237,121,205,169,112,22,80,2
37,120,203,127,40,250,237,120,203,
127,32,250,21,32,241,1,191,225,62
,14,237,121,1,191,255,237,89,1,19
1,255,62,15,237,121,1,191,255,22,
24,237,120,203,127,40,250,119,35,
237,120,203,127,32,250,237,120,20
3,127,40,250,237,120,203,127,32,2
50,237,120,203,127,40,250,237,120
,203,127,32,250,21,194,85,112,1,1
91,255,62,14,237,121,1,191,255,62
,255,237,121,251,123,214,2,95,0,0
,210,26,112,58,8,92,230,95,254,83
,32,7,58,8,92,230,95,32,249,205,2
09,112,58,8,92,230,95,254,66,194,
21,112,201,1,191,255,62,15,237,12
1,1,191,255,237,120,230,64,32,250
,62,1,205,203,112,237,120,230,64,
32,239,237,120,230,64,40,250,201,
245,241,61,32,251,201,221,33,0,88
,33245,112,17,32,0,14,32,6,24,221
,229,126,47,230,56,221,119,0,221,
25,35,16,244,221,225,221,35,13,32
,233,201,26,-1
```

This program will generate onto tape the necessary machine code program to run the Spectrum Freezer which can then be loaded as"FREEZER"CODE

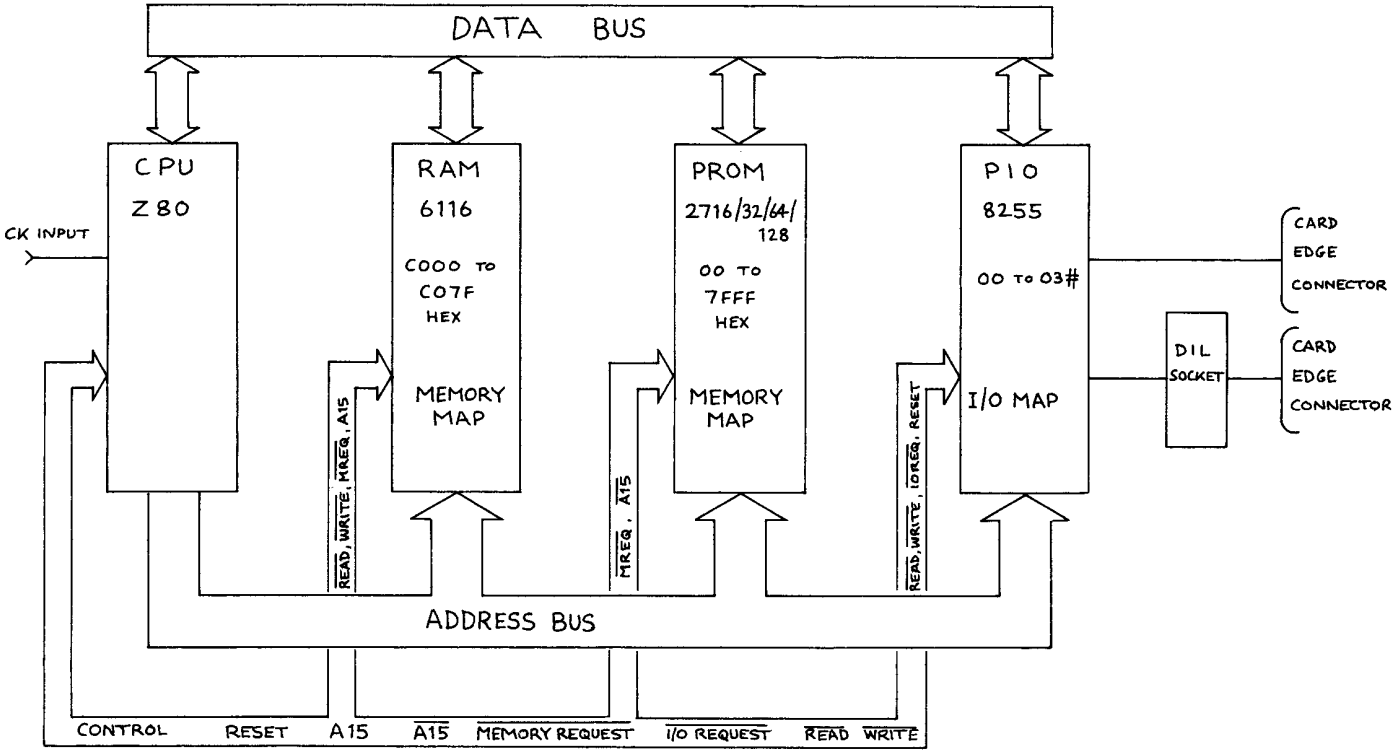
TELETRON

TELETRON is a micro controller for which a printed circuit card is available, designed to the new BATC card standard, i.e. ISEP with the artwork kept within Eurocard confines and a Eurocard edge connector, in order that the board can be cut to Eurocard size.

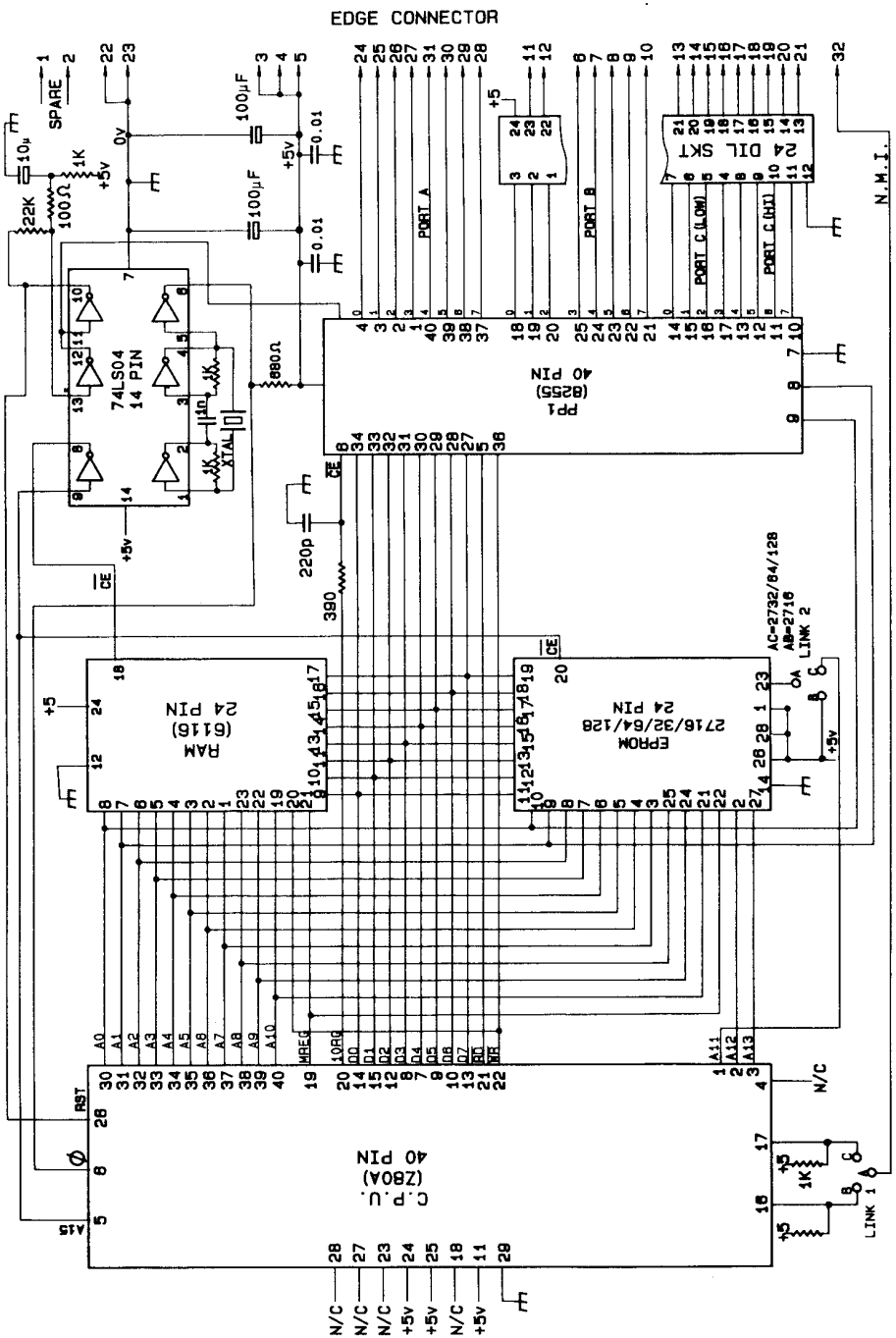
Micro controllers differ from computers in that the memory is made up largely of PROM with only a little RAM. The programme is stored in PROM so that at switch-on it is ready to work without the programme having to be loaded from keyboard or tape. Micro controllers do not usually have keyboards, VDU's or even a resident language. The programs are written in machine code with the aid of a development system and are then stored in Eprom and simply plugged into the controller.

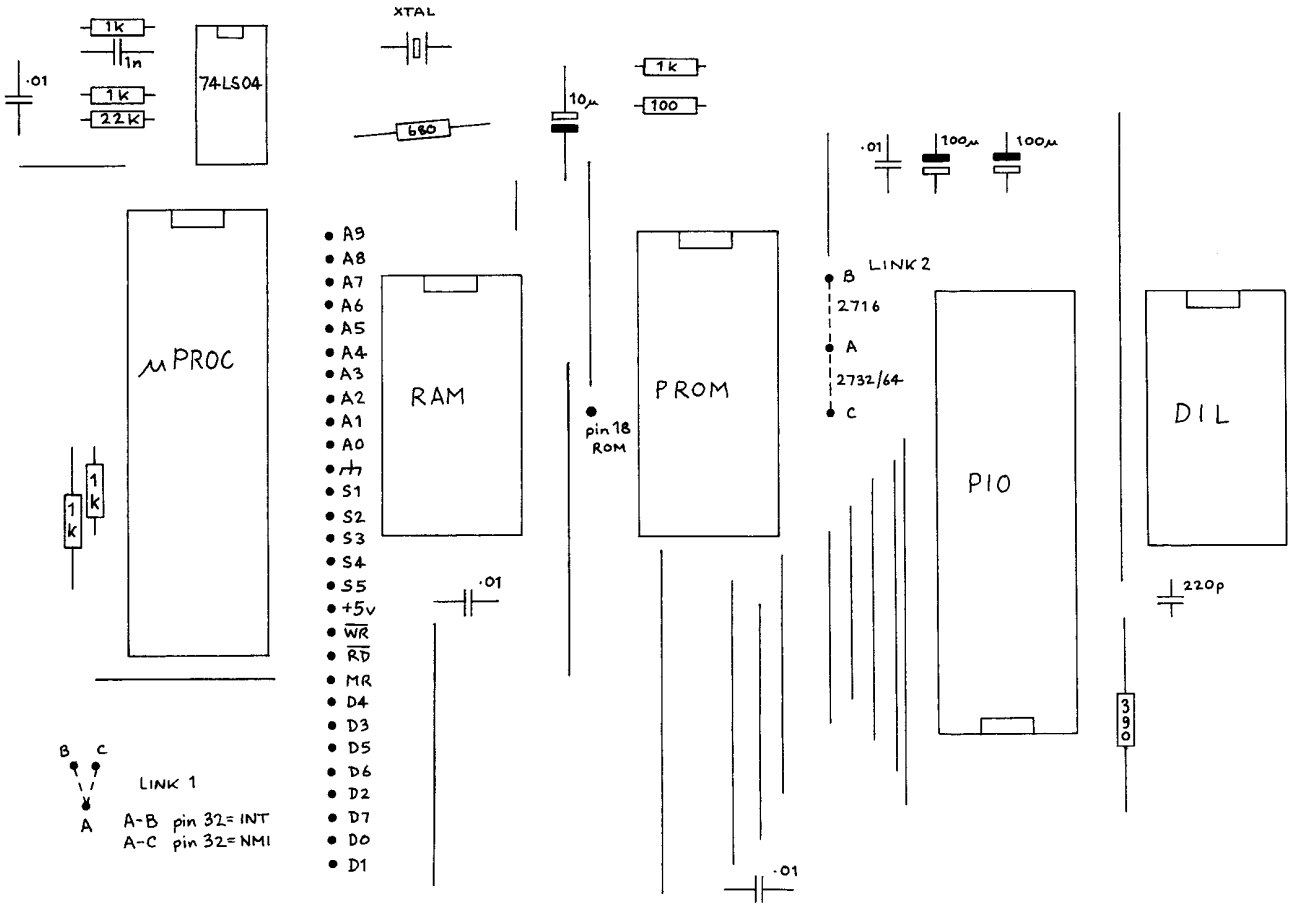
TELETRON uses a Z80A microprocessor and a 8255 PIO which provides 24 input/output lines. It has 2k of RAM provided by a 6116 and takes a single Eprom which can be a 2716, 2732, 2764 or 27128, depending on program size. Teletron has a 24 pin DIL socket which enables small 'piggyback' printed circuit boards to be installed along with the appropriate Eprom in order to dedicate the module to a specific task, e.g. a slow scan test card, or teletext generator or even the control logic for a TV repeater. By introducing a computer module in this way it is hoped to benefit from the advantages of computer technology without getting involved in heavy computer engineering. Teletron is the most flexible card module that we have yet introduced and it is hoped that many of these modules will be of use in the shack.

For the computer minded, Teletron has Eprom memory starting at 0000 hex and RAM at 8000 hex to 87FF hex. The programmable input/output chip (PIO) is located in the I/O map at locations 0 to 3 for ports A to D respectively. The DIL socket is connected to the PIO on pins 1 to 11 and to the card edge connector on pins 13 to 23 with ground on pin 12 and +5v on pin 24. The remainder of the PIO lines are all available on the card edge connector. Pin 32 of the edge connector can be connected to either INT or NMI by moving a link on the card, both INT and NMI are kept high by 1k pull-up resistors so they default to a non-active state.


DATA BUS
CPU
Z80
CK INPUT
RAM
6116
C000 TO C07F HEX
MEMORY MAP
PROM
2716/32/64/128
00 TO 7FFF HEX
MEMORY MAP
PIO
8255
00 TO 03#
I/O MAP
CARD EDGE CONNECTOR
DIL SOCKET
CARD EDGE CONNECTOR
READ, WRITE, MREQ, A15
MREQ, A15
READ, WRITE, IOREQ, RESET
ADDRESS BUS
CONTROL
RESET
A15
A15
MEMORY REQUEST
I/O REQUEST
READ
WRITE

TELETRON


EDGE CONNECTOR
SPARE
22K
100Ω
1K
10µ
+5v
0v
100µF
0.01
74LS04
14 PIN
XTAL
880Ω
PORT A
PORT B
PORT C(LOW)
PORT C(HI)
24 DIL SKT
N.M.I.
PPI
(8255)
40 PIN
220p
390
CE
RAM
(6116)
24 PIN
EPROM
2716/32/64/128
24 PIN
AC-2732/64/128
AB-2716
LINK 2
LINK 1
C.P.U.
(Z80A)
40 PIN
RST
A15
N/C
1K


1k
1n
1k
22k
.01
74-LS04
XTAL
680
10µ
1k
100
.01
100µ
100µ
µPROC
RAM
PROM
PIO
DIL
LINK 2
B
2716
A
2732/64
C
pin 18
ROM
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
S1
S2
S3
S4
S5
+5v
WR
RD
MR
D4
D3
D5
D6
D2
D7
D0
D1
1k
1k
.01
.01
220p
390
B
C
A
LINK 1
A-B pin 32= INT
A-C pin 32= NMI

TELETRON VDU

Because micro controllers do not normally have a VDU, that does not mean that one cannot be added. The most single desirable feature of this VDU is that it locks to a feed of external syncs. The characters it produces are large enough to be seen over an ATV link, making it possible to radiate captions or beam headings (useful if Teletron is controlling your aerial rotator).

The VDU format is 16 characters per line with 7 lines of print. The characters are produced by a 74276 character generator chip which pre-sets the character Fonts. The character borders are put in by hardware so graphics are not possible. The circuit has been kept as simple as possible, but because of the external sync feature, discrete logic has been used rather than the popular CRT controller chips, which would have resulted in a lower chip count. A small printed circuit board is available for this project, which eases construction.

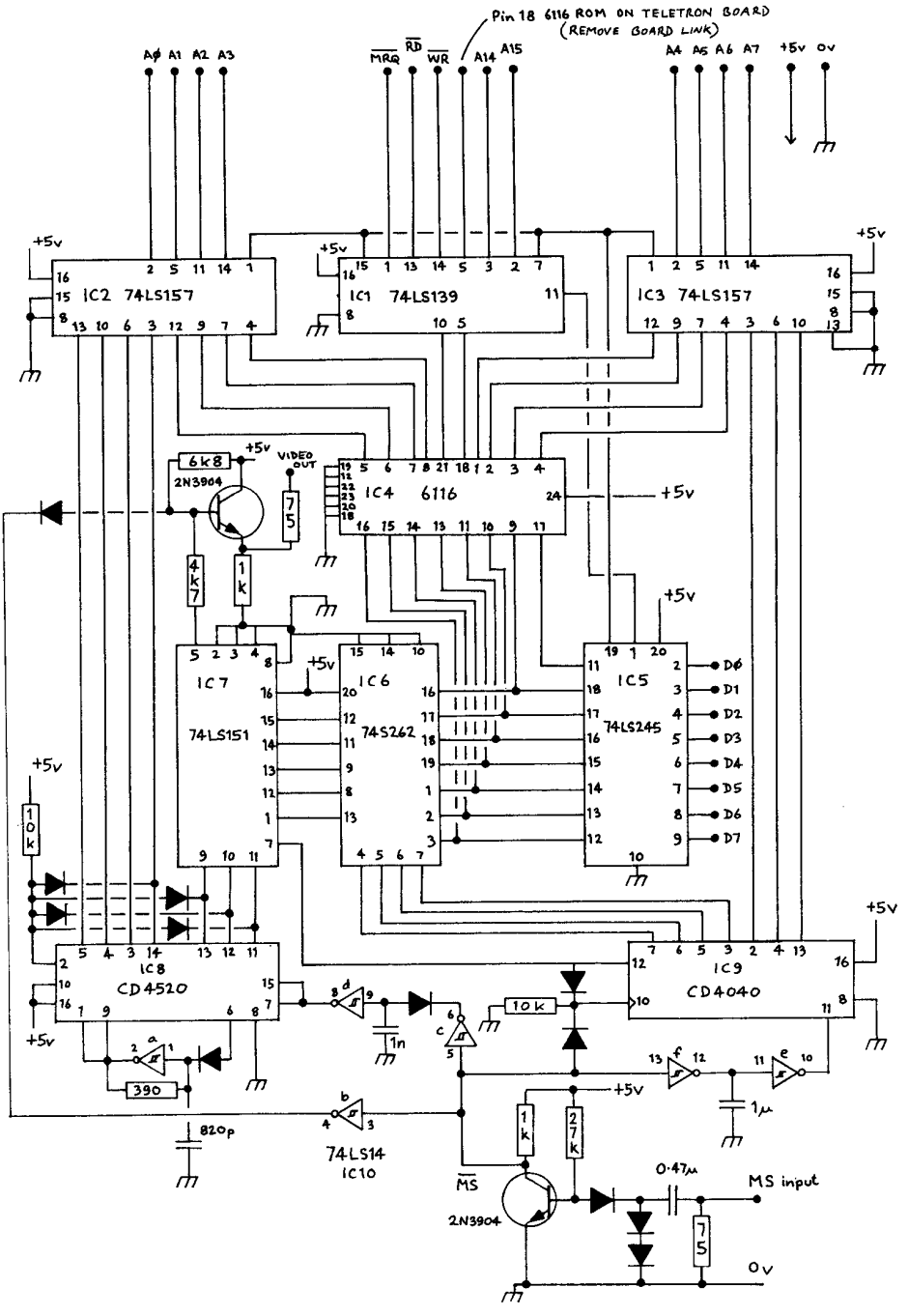
Teletron's VDU is memory mapped and resides in memory at C000hex to C07Fhex. The VDU produces 8 lines of text, but for reasons of circuit economy, the top line of text is in frame blanking and should not be used. The top line of text should be blanked out by loading memory locations C000 hex to C00F hex with 20 hex. The Fonts are shown in Fig.1 along with their ASCII codes.

The VDU can be read from, as well as written to, there is a little spare VDU memory at locations C080 hex to C0FF hex which can be used, but writing to and reading from VDU memory causes momentary disruption of the CRT display.

IC9 is a dual 4 bit synchronous binary counter wired as a single 8 bit counter. It is clocked by an oscillator comprising a single inverting gate (part of IC10), a 390 ohm resistor and an 820pF capacitor. The oscillator runs at a little over 2.5MHz, when the counter is full the diode on pin 6 causes the clock to stop until the counter is reset by line sync.

The outputs from this counter provide column address information for the 74151 which converts the columns supplied by 74S262 (IC6) into serial data, this counter also provides read addresses for the characters stored in IC4 (screen memory). IC9 is a large ripple counter which is clocked with line sync and reset with frame sync from the integrator comprising 2 gates from IC10 and a 1uF capacitor. This counter also uses a diode to inhibit counting when it is full (pin 12 to pin 10). This counter provides row addresses for the 74S262 and read addresses for the memory. When IC9 has finished counting it also stops IC7 from generating any unwanted repeat characters by lifting its strobe input. All the address lines from the counters are routed through two 74157 (data selectors) to the screen memory address pins, in order that the micro's address bus may be routed through to the memory to enable the micro to write, and in some cases read, from IC4 (screen memory).

IC1 is used to decode address information from the micro and switch the address selectors when the micro requires access to screen memory. IC5 is a bi-directional buffer controlling access to the screen memory data lines, this chip is also switched by decoded address information. TR1 combines the serial data from IC7 with incoming mixed sync to make a composite video signal. TR2 is used to buffer the incoming mixed sync signal

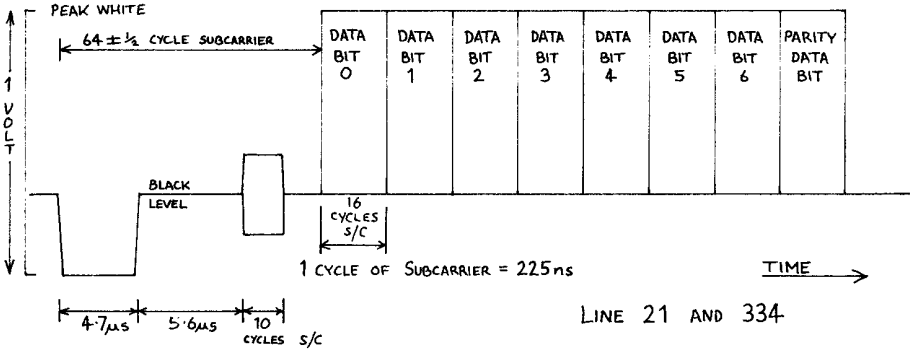

Pin 18 6116 ROM ON TELETRON BOARD
(REMOVE BOARD LINK)
A0 A1 A2 A3
MRQ RD WR A14 A15
A4 A5 A6 A7
+5v 0v
IC2 74LS157
IC1 74LS139
IC3 74LS157
IC4 6116
6k8
2N3904
VIDEO OUT
75
4k7
1k
IC7
74LS151
IC6
74S262
IC5
74LS245
D0 D1 D2 D3 D4 D5 D6 D7
10k
IC8
CD4520
IC9
CD4040
390
1n
10k
1µ
820p
74LS14
IC10
MS
2N3904
0·47µ
MS input
0v

HAM TEXT

There has long been a need for a system of vertical interval data that is not as complex as the current broadcast system.

A system is required which is a little more robust, in that it will work over the noisy paths often encountered by amateurs and that can be used with home video recorders or via amateur TV repeaters, or indeed by repeaters to acknowledge and log users. Repeaters could be extended to include limited mail box facilities such as a page on which skeds could be requested, this could be displayed after "time out". Repeaters that employ directional receive aerials could be given beam heading information. The possibilities are endless.

The following system fits one eight bit data word into line 21 (and line 334) of a standard TV picture. The first seven bits make up an ASCII word and the eighth bit is reserved for parity. This is a relatively slow data transfer speed which can easily be accommodated by a home micro which often uses a Basic program. The circuit is configured to plug straight into the rear socket of a Spectrum computer. The rear edge connector of a Spectrum is laid out with the Z80 connections so, with a little ingenuity, this system could be easily interfaced to any home micro - especially a Z80 based system.



The system protocol is such that only one page of data is sent and this is displayed as it is received with a "?" where parity errors exist. The page can be sent more than once if desired and dependent upon its prefix it can refresh the screen completely or just fill in any errors. Graphics are possible with this system and are transmitted as codes 00hex to 1Fhex with the exception of :-

02 STX
03 ETX
0A LF
06 ACK

If STX is sent then the screen is cleared and the text and graphics build up from the home position (top right of screen). LF signals the start of a new line. In the absence of an LF signal a new line is assumed after 32 characters. ETX signals the end of data and no further up-dating of the screen is allowed until an STX is received. The only exception to this rule is a 'repeat' message which commences with ACK and is stored in the computer in order that it may be compared with that on the screen and replace any displayed "?"'s due to incorrectparity.

VIDEO PORT

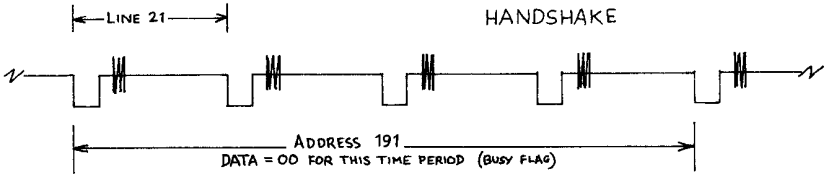
The video port has three functions:-

1) To strip mixed syncs from the video present at the video input in order to service the line 21 detection circuitry.

2) To strip line 21 data from incoming video and supply it to the RX data input on the shift registers.

3) To superimpose the data present at the TX output of the shift registers during line 21.

The sync separator comprises TR1, TR2 and TR3, TR1 being a DC restored stage which arranges that TR2 only conducts during negative sync excursions of the video signal. TR3 is necessary to restore the signal to its correct polarity and buffer the output. TX data is inverted in IC10c and then used to switch between incoming video and a DC level set by RV1. Switching is done in IC1 which is an analogue gate capable of handling linear signals such as video with very little picture degradation. TR4 and TR5 form a video output stage to restore the video to a one volt signal into a 75-ohm impedance. IC2 is a line receiver configured as a data slicer which detects when the video signal exceeds 0.5 volt and delivers a TTL logic 0. This signal is inverted at IC10d and fed to the shift register RX input.

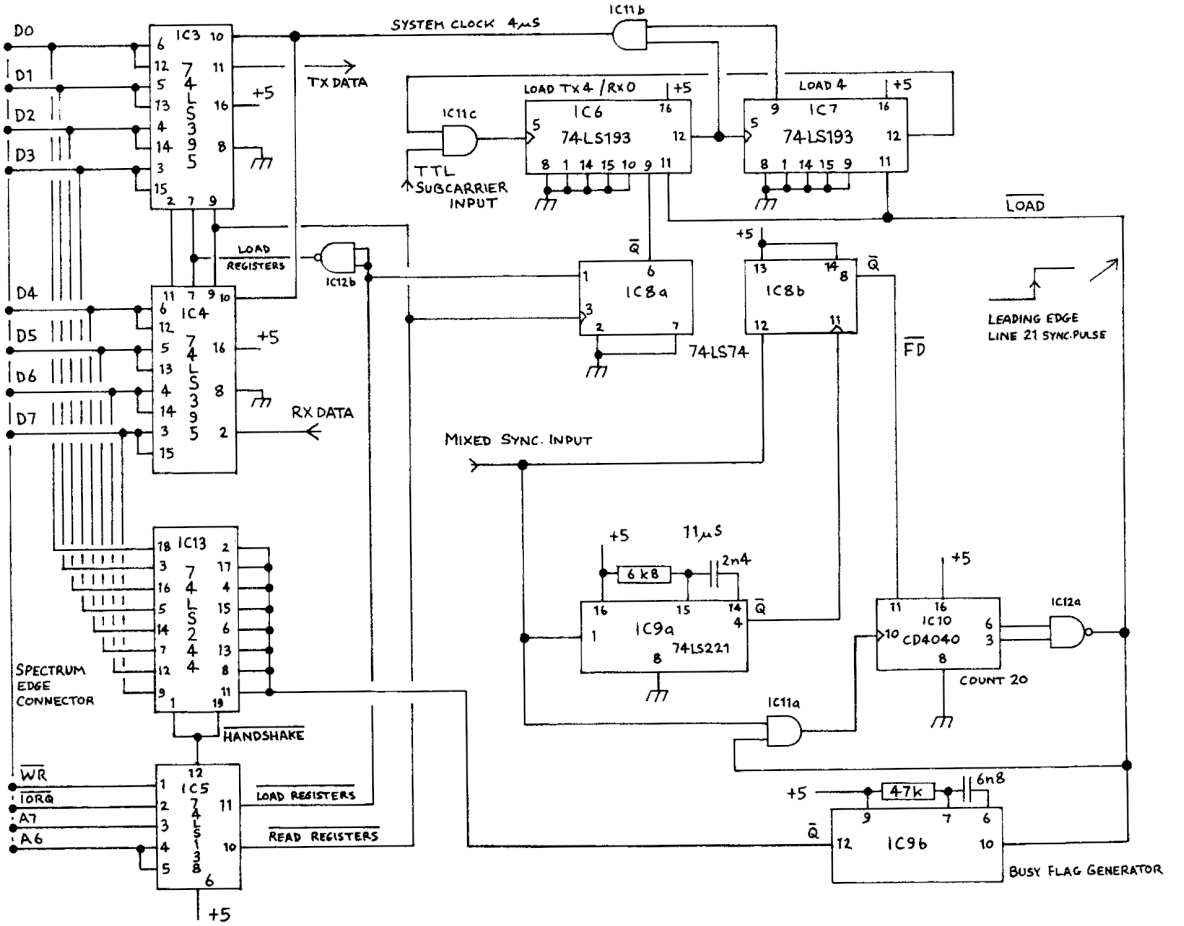


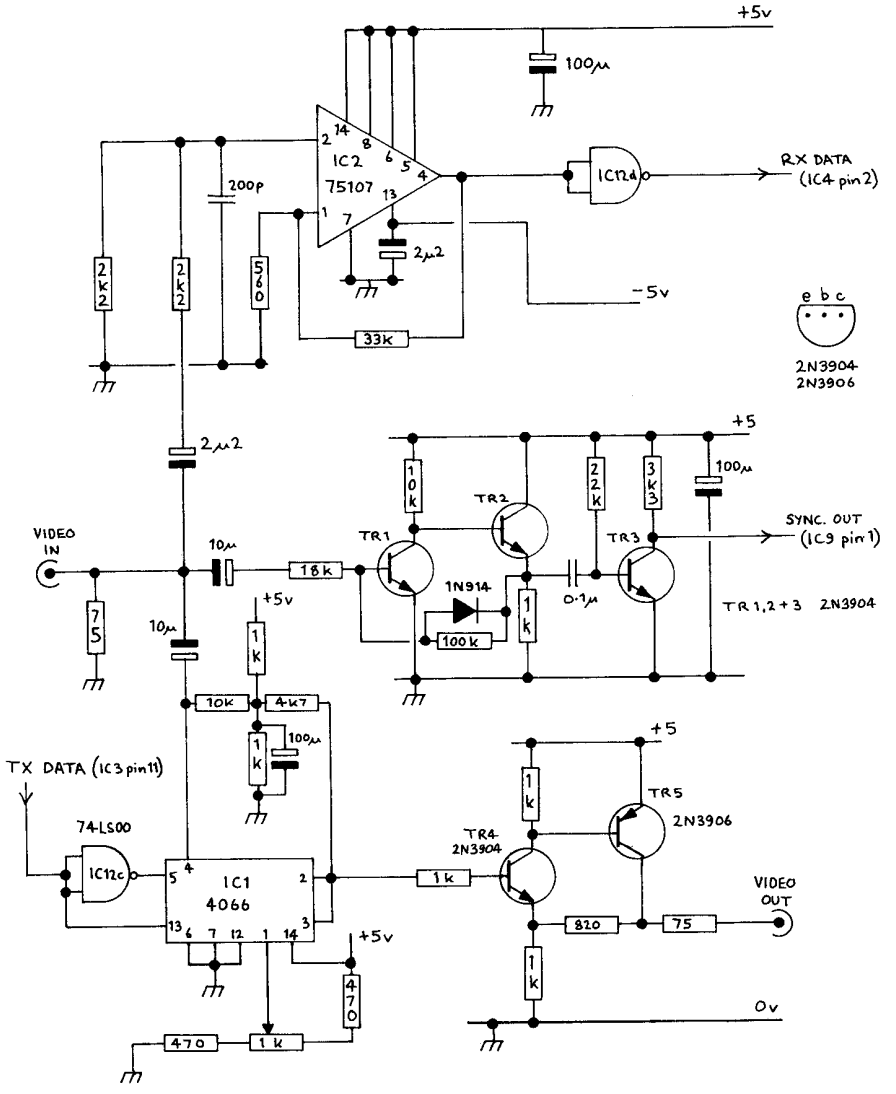
LOGIC BOARD

IC3 and IC4 are two-bit shift registers cascaded in order to cope with an 8 bit data word. They can be serial or parallel loaded and have parallel outputs via tri-state buffers, enabling them to be connected directly to the computer's data bus. IC5 is used to decode the read/write input/output request lines and address bus. This information is used to decide whether the computer is loading data fortransmission or reading incoming data, and configures the circuit accordingly. When a 'read request' is present the tri-state buffers within IC3 and IC4 are enabled and the data word stored within is presented to the computer data bus. When the 'write' command is generated, the data word is loaded into the shift registers.

IC6 and IC7 are two loadable counters which are used to generate pulses for the sideways shifting of data into and out of the shift registers. They are clocked with a free running subcarrier oscillator, but are held in load and only allowed to run during line 21. This simple logic will allow the position of the data to vary by 220ns, and as each data block is more than 4 micro seconds long problems should not arise.

IC9A and IC8B are a vertical interval detector. IC9A is a monostable with an unstable period of 11 micro seconds triggered by the leading edge of mixed sync. At the end of its unstable period it clocks IC8B (a D-type flip flop), which is looking at its D input for a low at this point in the mixed sync, (broad pulses). The waveform present at its Q is field drive, and the inverse of this is used to reset IC10 - a 12-bit counter.


D0
D1
D2
D3
D4
D5
D6
D7
IC3
IC4
74LS395
+5
TX DATA
RX DATA
SYSTEM CLOCK 4μS
IC11b
IC11c
LOAD TX4 / RX0
IC6
74-LS193
LOAD 4
IC7
TTL SUBCARRIER INPUT
LOAD REGISTERS
IC12b
IC8a
IC8b
74-LS74
LOAD
LEADING EDGE LINE 21 SYNC PULSE
FD
MIXED SYNC. INPUT
IC13
74LS244
SPECTRUM EDGE CONNECTOR
HANDSHAKE
WR
IORQ
A7
A6
IC5
74LS138
LOAD REGISTERS
READ REGISTERS
11μS
6k8
2n4
IC9a
74LS221
IC10
CD4040
COUNT 20
IC12a
IC11a
47k
6n8
IC9b
BUSY FLAG GENERATOR



HAMTEXT VIDEO PORT

IC10 is clocked with mixed sync. Once the 'load' is removed, it will be advanced until the count reaches 20, at which point the count is arrested by an AND gate IC11A. The count of 20 is coincident with the leading edge of sync prior to line 21. At this point the load command is removed from counters IC6 and IC7 which start producing 4 micro second pulses from the feed of subcarrier. The first 4 pulses are suppressed to give a 16 micro second delay and then the next 8 pulses start shifting data either into or out of the shift registers.

In the send mode data has already been parallel-loaded into the shift registers and requires shifting out of the TX end and onto the video port for superimposition on line 21 of the picture. In the receive mode the 8 clock pulses shift the incoming data supplied from the video port into the registers ready to be read by the computer. IC8b is used to detect and store the send or receive mode by being set or cleared by IC5's decoded commands. The Q is used to load a count of 8 into IC6 when a send operation is in progress and a count of zero when a receive operation is in progress. This advances the phase of the shift clock by 90 degrees in the receive mode to ensure that the negative clock edge, which shifts the
data, occurs in the centre of a data block.

Monostable IC9a is triggered from the leading edge of the line 21 detector and has an unstable period equal to a duration of approximately 4 lines. The purpose of this is to provide a handshake back to the computer to prohibit the same data word being read twice or the shift registers being reloaded before the word has been transmitted. After each data word has been read or loaded by the computer it signals the A6 line low and looks for 00 on the data bus. 00 is put on the bus by IC13 during IC9B's unstable period. When the computer has detected 00 it waits for it to clear before reading or writing to the shift registers again. Because the computer looks for 00 at address 191 to detect that it is safe to use the data bus, it does not get confused when 00 is put into the shift registers as graphic information.

Any communication concerning the contents of this book may be addressed to:-

Trevor Brown G8CJS
25 Gainsbro Drive,
Adel,
LEEDS LS16 7PF.
England. Tel: 0532 670115

If a written reply is required, please enclose a large stamped, self-addressed envelope or, for overseas readers, an I.R.C.

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2.3GHz Loop Yagi, 44 element, 2 metre boom, 22dBi gain (minimum), similar construction to 1.3GHz version.
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