THE ATV COMPENDIUM

Mike Wooding, G6IQM

BRITISH AMATEUR TELEVISION CLUB

BRITISH AMATEUR TELEVISION CLUB

THE ATV COMPENDIUM

Mike Wooding, G6IQM

ACKNOWLEDGEMENTS

The author wishes to express his gratitude to the following for their major contributions to this book:

Trevor Brown, G8CJS who supplied most of the circuits in the video section.

Bob Platts, G8OZP for the technical details of the 10GHz transceiver.

John Wood, G3YQC for the Universal Sync Generator.

Peter Delaney, G8KZG for the Digital Framestore.

Acknowledgement is also made to the following for information and assistance.....

Klaus Hirschelmann, DJ700. G.Wehrhahn, DD9DUK. Bill Brown, WB8ELK. Steve Mitchell, G8JMJ. Chris Smith. David Stone.

.....and also to the authors of works to which reference has been made, to the editors of other publications whose permission has been granted for reproduction of information, and to all those who have given advice and encouragement during the compilation of this book.

For information regarding membership of the BATC please contact Dave Lawton G0ANO, Membership Secretary, 'Grenehurst', Pinewood Road, High Wycombe, Bucks. HP12 4DD, enclosing a stamped addressed envelope.

First edition.

First printing March 1989.

Wooding, Mike: The British Amateur Television Club
The ATV Compendium

ISBN 0-9513779-1-4

CONTENTS

VIDEO CIRCUITS

SPECIAL PROJECTS

R.F PROJECTS

FOREWORD

For something approaching the past decade the BATC has been publishing handbooks, dealing exclusively with the world of Amateur Television. These publications have proved to be very popular with the membership throughout the years, prompting the club to reprint and update the material from time to time.

The last handbook the Club produced was the 'Slow Scan Companion', the first publication of its kind in the United Kingdom totally dedicated to Slow Scan Television. This handbook marked another landmark in the Club's history, in that it was the first of our publications to feature a full colour cover.

The ATV Compendium does not break any bounds in the club's publication record, but I hope it will serve to inform those interested in Amateur Television, particularly those of you involved in home construction. I have tried to include projects that include the use of 'state-of-the-art' techniques and devices, without precluding those who do not own sophisticated test equipment or have degrees in mechanical engineering.

There is one large omission from this book that I am sure will not go unnoticed, this is the lack of a 70cm section. Although this was certainly not intentional when I started, it soon transpired that the amount of material coming in for other topics , particularly 3cm, coupled with the absolute lack of anything new for 70cm, meant that for the first time an Amateur Television handbook without a section for the novelty sentimentalists would be the outcome. Also, with the vast commitment of time necessary by all involved with the production of a book like this, coupled with the economics of publishing books with greater page counts, had any material for 70cm been available I would have been in a difficult situation deciding what to leave out.

However, with the pressure being placed on 70cm these days, from inside the amateur world as well as outside, perhaps the time has come for us to place the emphasis on the higher bands. It is certainly true to say that working in amateur TV on the higher bands is exciting, offering the opportunity for experimentation in the true amateur spirit. There is a lot of work to be done in the area of wideband FM and high definition television, and I feel sure that the amateur world has a lot to offer the professionals, as has certainly been the case in the past.

Finally, I wish to offer my personal thanks to all those mentioned in the acknowledgements for their help. Also, special thanks go to John Wood G1YQC for his help with all the artwork, editorial advice and support during what appears to have been a very long year, and to Trevor Brown G8CJS for his support.

I hope that you find this book interesting, informative and above all, unoful.

Mike Wooding G6IQM.....Editor.

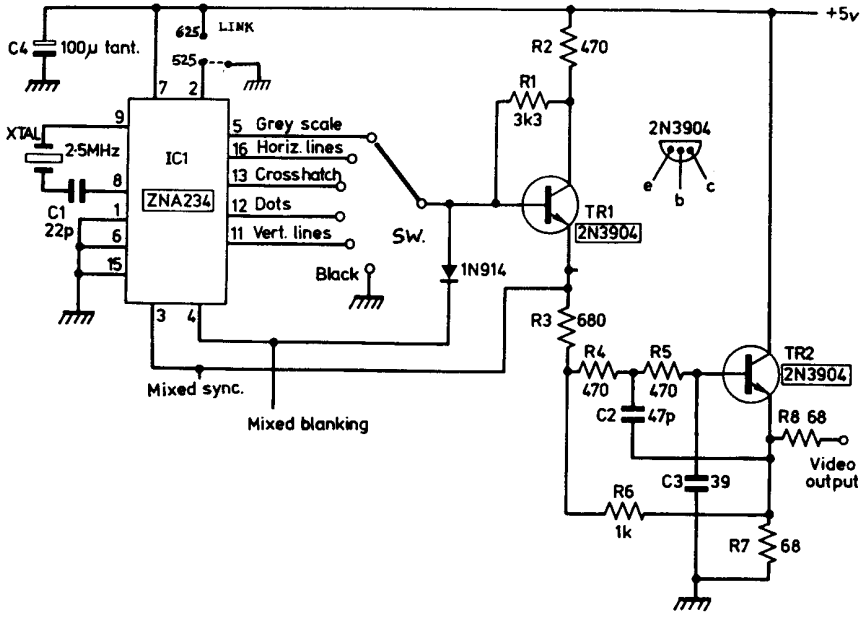
DUAL-STANDARD PATTERN GENERATOR

A useful aid in the ATV shack is a pattern generator, useful for setting up monitors, transmitters, VCR's etc. This circuit is built around the Ferranti ZNA234 television sync and pattern generator IC. The patterns available are grey-scale, horizontal lines, grille, dots and vertical lines. The grey-scale pattern is a descending one (ie: white at the left, through grey, to black at the right) rather than the more usual ascending one. This does not however affect its use as a test waveform.

The ZNA234 is a multi-standard device in that the line frequency is set externally by an appropriate crystal. For 625 lines the crystal frequency should be 2.5MHz and for 525 lines 2.18MHz. The number of lines per frame is set by the voltage condition on pin-2 of the chip, connecting it to +5 volts sets the frame rate for the 625 line standard, connecting it to 0 volts for 525 lines.

Transistors TR1 and TR2 provide the necessary buffering of the signal from TTL levels to present a composite 75-ohm video output. Mixed sync and blanking are available from pins 3 and 4 respectively at TTL levels, for driving additional equipment if required.

There is no printed circuit board available for this unit, but it can be simply constructed using Vero-board. As with the simple pattern generator described elsewhere no special attention needs to be paid to the layout of the components.



FOUR-INPUT VISION SWITCHER

An alternate circuit for a four-input vision switcher is described here using the TEA2014 device. This device features one video changeover switch and a separate non-switched output, in an 8-pin dual in-line package. In order, therefore, to provide our four input unit three of these devices are required.

CIRCUIT DESCRIPTION

The inputs are selected by pressing an appropriate push-button which should be a momentary type with an in-built LED. The circuit gives priority to the right-hand button (number 4) should more than one be pressed at once.

When a button is operated IC1, an 8-to-3 line encoder, generates a 2-bit code representing that button. This code is stored in a dual D-type (IC3) which is first cleared by IC1, thus ensuring that the correct code is stored. An inverter (IC2) is required between the output from the encoder at pin-15 and the clock inputs on the D-type, pins-3 and 11.

The code is then passed to a 74LS139 dual 1-of-4 decoder (IC4), which has the inputs to both halves paralleled together. One set of outputs from the decoder is used to switch on the LED's in the push-buttons and the other set used to control the vision switches. IC5's gates are used to buffer the decoder outputs and source the supply for the LED's in the push-buttons. Transistors are required to shift the voltage level from the TTL output of the decoder to the higher voltage required by the switching IC's.

The actual switching is carried out by the TEA2014 IC's (IC's 6 to 9) which are custom-built analogue vision switches. Each has two inputs; one via pin 3 having unity gain and the other via pin-8 having a gain of 2. To overcome the probability of non-standard video levels being presented to the switches, each input is via a 100 ohm potentiometer to allow all the input levels to be equalised at 1 volt p-p.

CONSTRUCTION

A printed circuit board has not been made available for this project as it is only offered as an alternative to the colour vision selector described elsewhere in this book. However, by carefully laying out the components on a piece of Vero-board a suitable unit could be built. Try to avoid crossing any video lines with others, and avoid placing the output adjacent to any input line. The push-buttons are numbered one to four on the circuit diagram with number four having the highest priority, and so on in reverse order down to number one. The power requirement is 12 volts, with the on-board 7805 regulator supplying the 5 volt rail for the logic. A suitable keyboard rocker switch is available from RS Components (Electromail) stock no: 337-374 (red LED) or 337-380 (green LED).

As suggested before, for a really 'professional' effect, the Fade-to-Black unit described elsewhere in this book should be installed between the switcher and the transmitter for smoother changeovers.

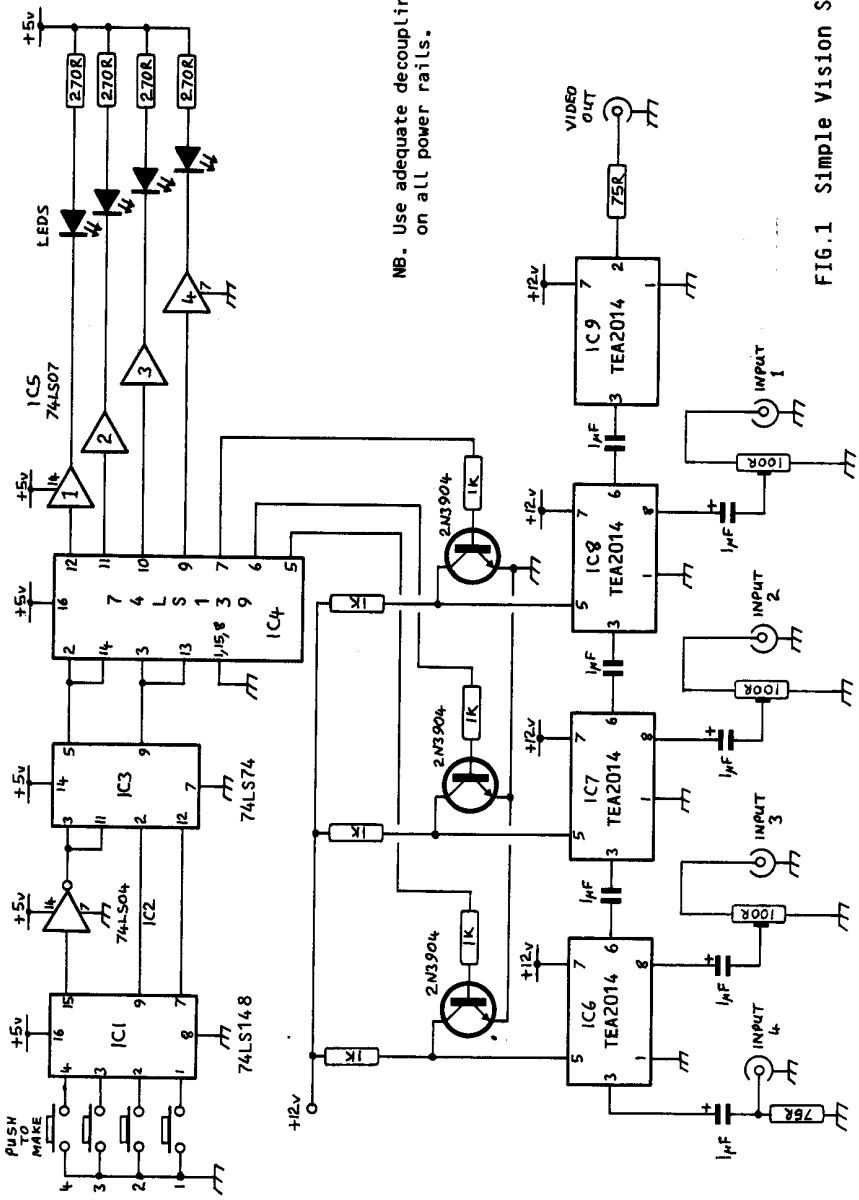


FIG.1 Simple Vision Switch

ELECTRONIC VISION SELECTOR

The electronic vision selector is a very useful piece of equipment in the shack. With a multitudinous array of vision sources available to the modern amateur, such as cameras, computers, caption generators, VCR's etc., the method of changing plugs and sockets to select sources is no longer very satisfactory. The circuit described here offers a simple and practical way of effecting changes between four vision sources. Switching is not field sequential.

The unit is based on the Thomson TEA5114 custom built analogue video switch. This device contains three separate changeover switches and a fast blanking switch. Each of the switches within the device features a stage gain of two, thus in this circuit each of the inputs will have differing sensitivities, which can be accomodated by the gain controls. Low level video sources less than 1 volt should be applied to inputs 1 or 2 in order to benefit from the maximum gain of the cascaded switches.

CIRCUIT DESCRIPTION

The switcher provides four inputs and uses simple non-latching push-buttons to select sources. A tally LED is also provided for each input, which is switched on whenever the input is selected. The push-button commands are coded into a two-bit code by the 74LS148 Priority Encoder, this ensures that if two or more buttons are pressed at the same time the higher number button takes priority. The code is then latched into the 74LS75 and stored there until another button is pressed, as well as being routed to both halves of the 74LS139 Dual Decoder. One set of decoded outputs is used to drive the tally LED's and the other to control the TEA5114 switching. Voltage level adjustment between the outputs of the decoder and the control inputs of the switches is achieved by the Zener diode and 1K resistor. The inputs have an impedance of 75-ohms, and each has a 100-ohm gain control in order to balance the sources to provide a 1 volt p-p output into a 75 ohm load.

CONSTRUCTION

A pre drilled printed circuit board is available from BATC Members' Services, this has a ground plane on the component side. Before fitting any components this ground plane should be removed from around the holes for components that do not connect to ground, using a small drill or Vero tool. The push-buttons as numbered on the circuit diagram give number four the highest priority and number one the lowest in the switching order. These switches may be either mounted direct onto the PCB, or remotely onto a front panel. Provision is also made on the PCB for the four 330-ohm resistors that pad the input down to 75-ohms, if remote input sockets are used these are best mounted at the sockets. A suitable keyboard rocker switch is available from RS Components (Electromail) stock no: 337-374 (red LED) or 337-380 (green LED.

It is suggested that for a really 'professional' effect, a Fade-to-Black unit be installed between the switcher and the transmitter, so as to give smooth transitions from one source to another. A circuit for such a unit is included elsewhere in this book.

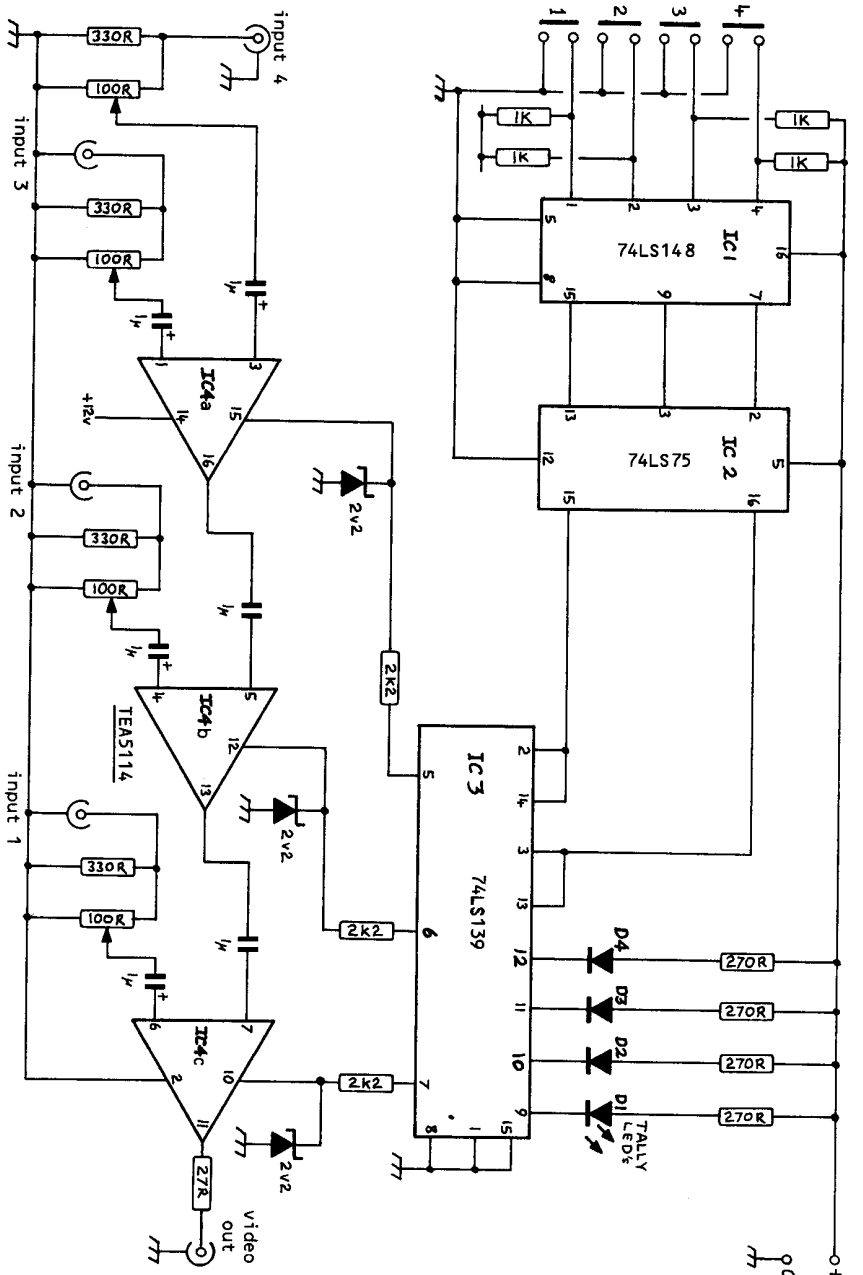


Fig.1 Four Input Colour Vision Selector

FADE TO BLACK

In order to effect a smooth changeover from one video source to another, the video should ideally be faded to black whilst the switching takes place. However, if the composite video source is simply faded down the sync pulses are also lost, and the resultant changeover suffers from loss of sync until the up-fade video signal is strong enough to lock the picture. Consequently, what is required is a unit that will fade the video but maintain the syncs. The two circuits described here do just that. In Fig.1 is shown a circuit using the TEA5114 device, and in Fig.2 using a TEA2014.

CIRCUIT DESCRIPTION

The incoming video signal is fed to the LM1881 Sync Separator IC, which extracts the sync pulses and the burst gate (if colour is being used). These two signals are then gated together by the TTL (74LS00) gate in Fig.1 and by the C-Mos (CD4081) gate in Fig.2. The logic signal at the output of the 74LS00 is inverted by TR1 (BC107) and fed to the switch control input. In Fig.2 the output from the C-Mos gate is too high for the control input of the TEA5114 video switch, so a 2.2K resistor and 2v2 Zener diode are incorporated to limit this to 2.5 volts.

The input video signal is also routed to the fader control, the output of which is fed to the normally open input of the video switch. The video is further routed to the normally closed input of the switch. During normal operation, without a fade, the video switch toggles between its two inputs, changing over from the input on pin-1 (pin-3 Fig.2) to that on pin-3 (pin-8 Fig.2) whenever the extracted sync control voltage is not present, and changing back again when it is. This toggling action is very fast and causes no disruption to the picture as the changeover actually occurs during the blanking period.

When the input video is faded down, during the time the switch is routed to the faded input (ie: between sync pulse trains) black level is routed to the output. However, during the sync pulse intervals the control voltage is again present and the switch changes to the non-faded input, thus presenting sync pulses and burst to the output. The end result of this is to give an output waveform containing normal sync and burst, but without any video information.

CONSTRUCTION

Due to the simplicity of the circuits, printed circuit boards have not been made available. The units can be easily built onto pieces of Vero-board and mounted directly onto the fader, if required. No particular attention need be paid to the positioning of the components. A single 12 volt power rail is all that is required.

NOTE: Early samples of the TEA5114 showed differences in the voltage levels of black level clamps at each input. This was overcome by adding the 100K resistor at pin-1. This has removed the problem in all units built so far, but if the problem persists a micro switch operated by the fader when in the non-fade position grounding pin-15 of the TEA5114 should be added. This would prevent the toggling action from taking place when no fade is present.

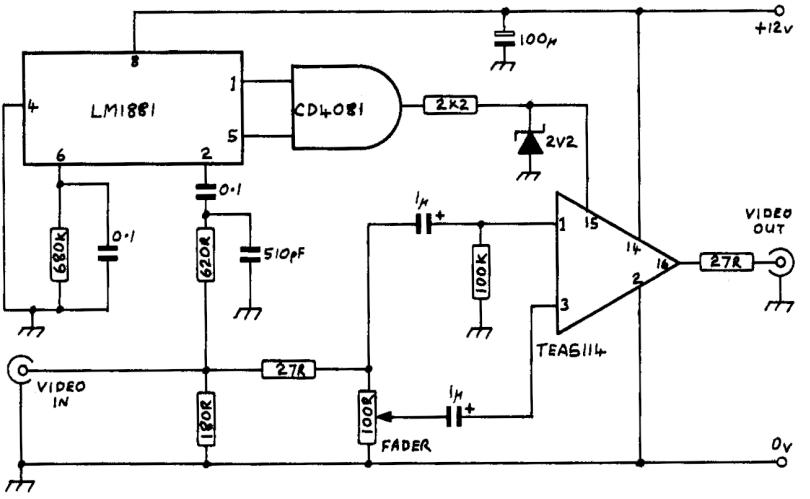


Fig.1 Fade To Black Circuit using TEA5114

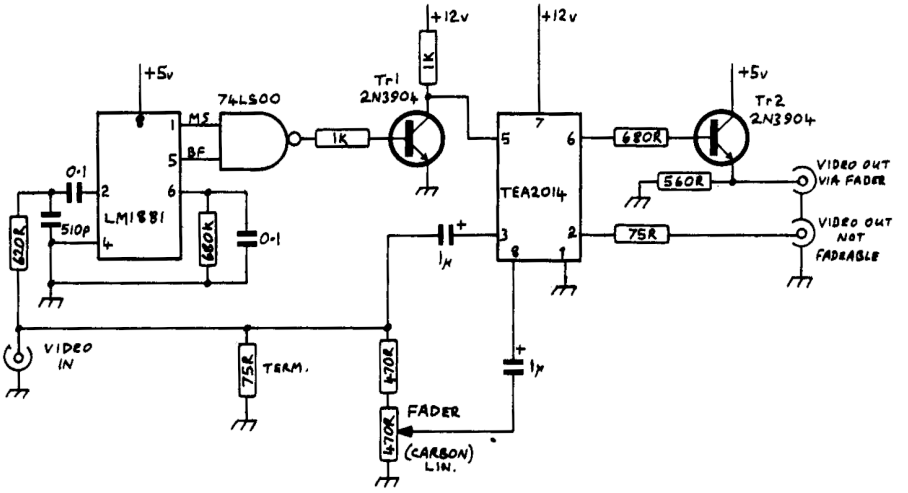


Fig.2 Fade To Black circuit using TEA2014

SUPERIMPOSING CAPTION GENERATOR

The circuit described here is a character generator that will superimpose its caption onto any composite video signal. The unit works at both 525 and 625 line standards without any adjustment or circuit changes. The display consists of one line of fourteen characters which should be enough for your call sign and name or locator details. The circuit requires a composite video input signal to which it will synchronise. This is then inset in the form of a black box with white characters inside. The character fonts are stored in an E-Prom which has to be programmed with call sign and station details. Two video outputs are provided; one containing the inlaid caption and the other without. The display can be located at either the top of the picture or in the middle, alternatively it can be made to repeat several times down the screen.

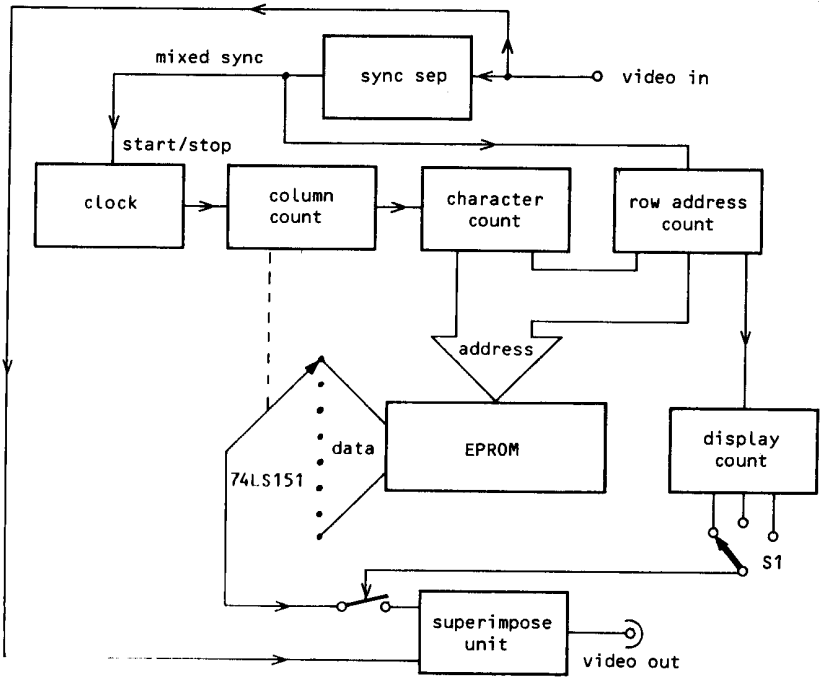


Fig:1 Block Diagram

CIRCUIT

A basic block diagram is shown in Fig.1 and the circuit in Fig.2. Incoming video is fed to an LM1881 sync separator IC (IC8) which strips off the video and routes the sync information to the dot clock

oscillator IC1. This oscillator runs at approximately two hundred times line frequency, and is synchronous to the incoming signal because it is stopped and restarted at the commencement of each scanning line. The dot clock is used to advance the column counter (IC3a), which generates an address that is incremented across the line and used to drive IC6, an 8-to-1 line data selector. IC6 scans across the data outputs of the E-Prom (IC5) and outputs a data stream to the data latch IC7a. This data stream represents the series of dots making up the top row of the first character.

The character counter IC4a is then advanced by the dot clock and with it the E-PROM address bus. IC6 now scans the E-PROM for the data information for the top row of the second character and sends the information to the data latch. This process is repeated until all fourteen characters have been scanned. The dot clock is stopped and restarted by the incoming sync information signalling the next scanning line. The row address counter IC4b is clocked by the incoming line sync and steps the E-PROM address bus through to the information for the next row of the characters, and the reading process repeated for the second row of each character. This entire process is repeated until all the character information has been read from the E-Prom. IC3b is the row counter and is advanced after each display. Switch S1 enables the counter to determine which lines are to be blanked out thus allowing the characters to be superimposed.

Data latch IC7 is required to clean up the dot stream and remove any false information from the ripple counters. The latch is clocked by the dot clock and its output routed to the video switch IC9. The characters are superimposed onto the through video by creating a 'black box' into which the characters are inserted. The black box is produced by clocking the video switch with a signal derived from the character row counter IC3b. When the TEA2014 is switched the character information is inserted into that picture line instead of the through video, thus building up a complete picture with the character information superimposed onto the video.

CONSTRUCTION

As with most of the projects in this book a printed circuit board is available from Members Services, please refer to your latest copy of CQ-TV for details. All the logic IC's should be 'LS' types, and are better mounted in good quality sockets. The E-PROM type shown in the circuit diagram is a 2716, however, the PCB has been designed to accommodate the larger 2732 and 2764 types. To facilitate this pin-23 has been left floating, for 2716 a solder bridge to the +5v pad should be fitted, for the other devices a solder bridge to ground. E-PROM types 2716 and 2732 should be fitted at the bottom of the socket, leaving locations 1, 2, 27 and 28 unused.

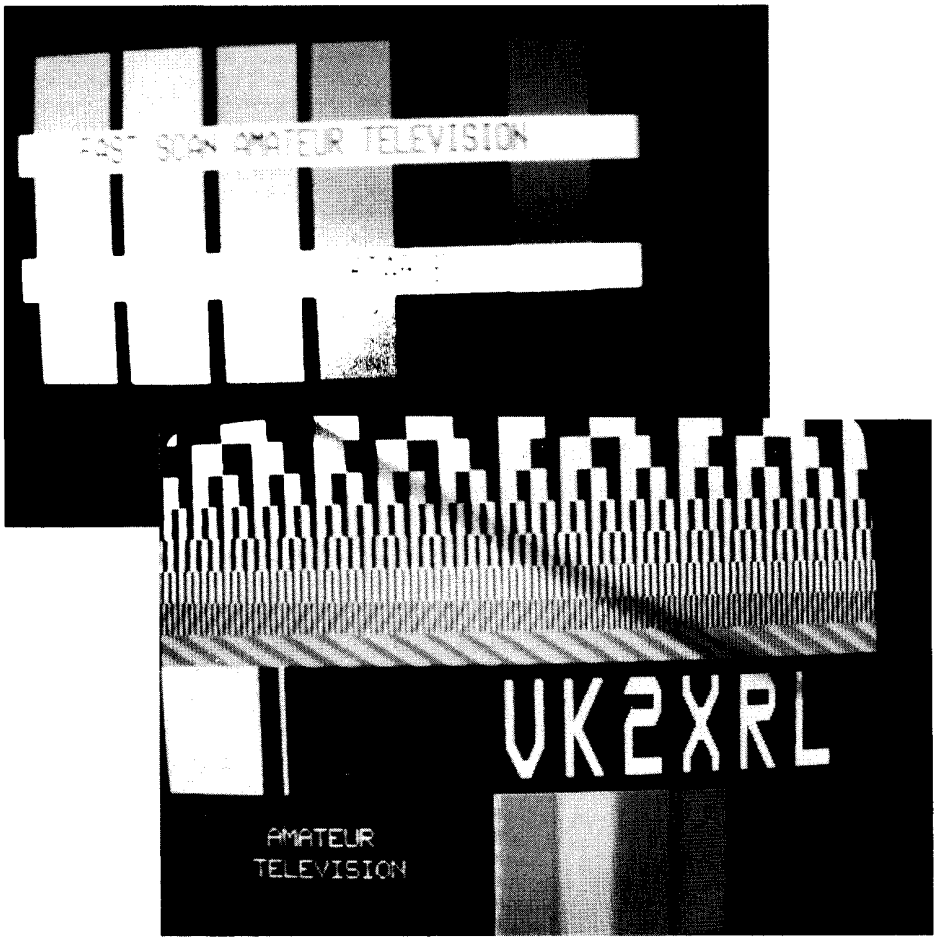
The video input requires terminating in 75-ohms. this has not been catered for on the PCB as some stations may require to switch it in or out to allow equipment to be looped together.

The connections for switch SW1 are brought out to solder pads at the edge of the board, as are the connections for RV1. These leads will be carrying signals at TTL levels and should not be longer than eight inches. this would allow connections to the front panel of an enclosure to be made.

The sync separator chips may be available from Members Services, please check your current copy of CQ-TV, alternatively, they are available from Farnell Electronics at the address shown below. Programmed E-PROMS are available from BATC Members Services, please quote the call sign and name or locator required when ordering.

The only setting-up required is the level of the superimposed characters, which is achieved by adjusting RV1 until the desired balance is obtained between the characters and the through video. The regulated power supply should be 12 to 15 volts and be capable of delivering 500mA.

Farnell Electronic Components, Canal Road, Leeds LS12 2TU.
Tel: 0532 63611



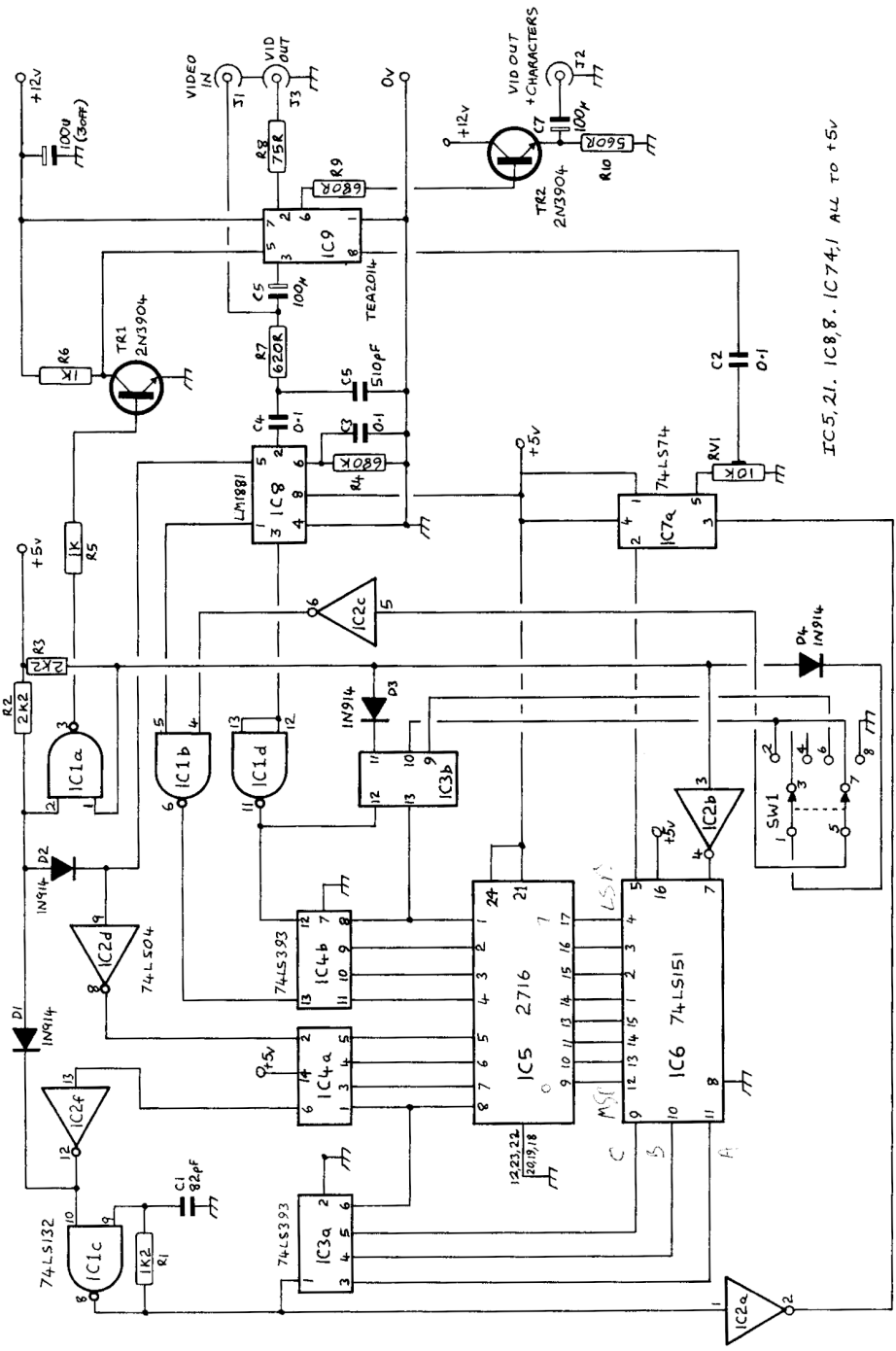


Fig.2 Video Character Generator

ELECTRONIC AMATEUR TEST CARD

The electronic test card generator described here is based on the original design which appeared in Radio and Electronics World in July 1983. This circuit encompasses all the patterns provided by the two simple circuits described elsewhere in this book, plus extra important test signals to enable the correct setting of equipment. The test card has the added advantage of providing station identification and of being in colour. The colour content can be coded to the correct format for either the PAL or NTSC systems, and the whole unit requires only a single 12 volt supply. The pattern information, call sign and station details are held in a 2732 type E-Prom which is read by the logic circuitry of the generator. A pre-drilled printed circuit board is available from BATC Members Services, the E-PROMs are available with a choice of several different patterns from the Worthing Repeater Group (see advertisements in CQ-TV).

As stated the test card pattern has all the features of the other generators in the one pattern and these include:

1) Grille pattern to provide a rough linearity check on the monitor scans.
2) Black rectangle within white to test the low frequency response, and white needle pulse to test for reflections.
3) 150KHz square wave to test transient response.
4) Up to eight bold characters for your callsign.
5) Multiburst bandwidth response test, producing 6uS bursts of 0.5, 1.0, 1.5, 2.0, 2.5 and 4.0MHz.
6) Colour bars to check the performance of a receiver decoder and the colour performance of any other units in the path, such as video switches, modulators, receivers and transmitters.
7) Two lines of up to twenty characters for your QTH, shack details or other message.
8) Optional BATC logo just to show that you are a member of the World's leading ATV organisation.

CIRCUIT

All the circuit timings are derived from a crystal oscillator (x1) which runs at 7.781MHz for 525 line working and 8MHz for 625. The oscillator uses two logic gates (IC2) biased as amplifiers, and this provides the video dot rate. The clock also drives the counter IC1 where it is divided down to 1 and 2MHz, the outputs from the counter provide the character clock and control signals.

The 1MHz clock drives the address counters IC3 and IC4, which are incremented for each character cell on the display for the 64 character row addresses. In each character cycle the address of the character is latched through a multiplexer into IC5, IC6 and IC7. The character corresponding to this address is read from the E-PROM (IC8) multiplexed, and then latched back into the E-PROM address along with the character scan line number from the address counter. This address gives the character number and scan line number for the character generator, which is also contained within the E-PROM.

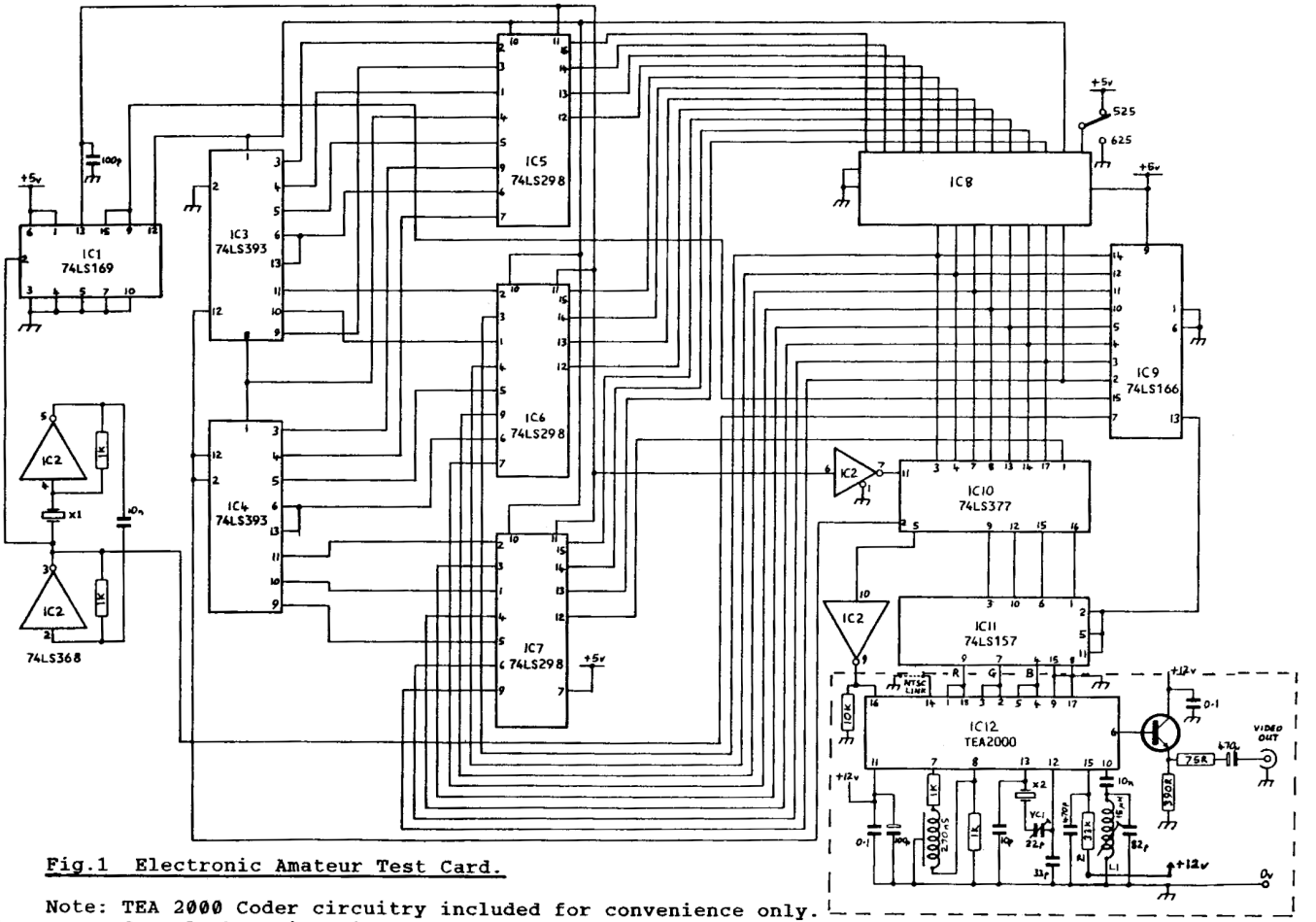


Fig.1 Electronic Amateur Test Card.

Note: TEA 2000 Coder circuitry included for convenience only. See elswhere in this handbook for details.

The data output then forms the dot pattern which is converted into serial form by shift register IC9, and routed to the video circuitry. If when the character is read from the E-Prom the data bit is set, then the dot pattern when read is latched by IC10 instead of the shift register IC9. The output from IC10 is then used to control the colour coder chip IC12, reset the address counters and generate synchronisation pulses.

The reset pulse is used to return the address counter to zero at the end of each frame. Because of this the number of lines per frame is controlled by the E-PROM, thus it is necessary to program each E-PROM with both a 525 and a 625 test pattern. To select which pattern is required it is simply necessary to alter the logic state on A12 at pin-2 of the E-PROM, grounding the pin will select the 625 card, connecting it to +5 volts will select the 525 one. A PCB pad is provided at pin-2 of the E-PROM to enable this selection to be made easily.

The colour coder is contained within a single chip the TEA2000. This device is capable of encoding to NTSC or PAL standards by either grounding pin-14 for NTSC, or leaving it 'floating' for PAL. The crystal connected to pin-13 (x2) needs to be twice the frequency of the colour subcarrier, ie:8.867MHz for PAL and 7.1276MHz for NTSC. L1 should be adjusted for maximum subcarrier and the burst position may need altering between standards, this is done by changing the value of R1. The delay line at pin-8 should be a 270nS type (Philips V8470 270nS/900-ohm), as found in domestic TV sets.

The three D-A signals are multiplexed with the black and white signal in a quad 2-line to 1-line multiplexer (IC11). The resulting RGB signals are fed to the colour encoder IC12. The coded output is taken from pin-6 and is buffered by a simple video amplifier circuit providing a composite video output at 1 volt p-p across 75-ohms.

CONSTRUCTION

The pre-drilled PCB makes construction quite easy. Ensure that all the through-board wire links are soldered on both sides, as well as any components and IC leads that connect to both sides. Fit the correct frequency crystal for the standard you require and use good quality components throughout. The link at pin-2 of the E-PROM should be set for the test card required, as should the link at pin-14 of the coder for the system standard. The coder is quickly set up; adjust L1 for the maximum level of subcarrier and VC1 for correct locking of the colours (subcarrier frequency).

The 12-volt supply rail should be adequately regulated and be capable of supplying of the order of 500mA, all the logic circuitry is supplied from the on-board 7805 regulator. A heatsink should be fitted to the regulator device, this may be an on-board type but consideration must be given to the quite considerable heat generated when mounting the unit in a cabinet. It may be more suitable to mount the 7805 device off the board on a separate heatsink and feed the regulated +5 volts back to the circuit.

For details of ordering the PCB and E-PROMS please refer to the Member's Services and Worthing & District Repeater Group advertisements respectively in your current copy of CQ-TV.

VIDEO DISPLAY GENERATOR

This project has been included in the handbook specifically for our American members. The unit is designed to work to the 525 line NTSC standard, and as such is not suitable for use outside the USA.

The Elektronics VDG-1 Video ID board is a self contained module that will produce a quick source of computer video upon applying power. Four computer generated graphics screens are stored in a 27C128 E-PROM, two high-resolution screens and two colour bar patterns are available. These screens are located within different areas of the E-PROM's memory and are selected by controlling several address lines by means of four single-pole/double-throw switches wired to positions SW1 to SW4 on the printed circuit board. The output from the unit is standard 525 line NTSC at a level of 1 volt peak-to-peak, which can be connected direct to your ATV transmitter input, video monitor or video recorder. There is also a video relay in the circuit which routes live video through when the power is turned off. To identify your transmission, or for use as a test pattern, just turn on the ID board and the relay will switch from the through video to the generated picture. Finally, an automatic sequencer/timer featured in the circuit allows you to sequence through all four screens, or several combinations of two screens, varying from 0.2 seconds per screen up to a maximum of one minute per screen.

CIRCUIT DESCRIPTION

The circuit diagram of the unit is shown in Fig.1 The clock frequency to drive the 6847 Video Display Generator (VDG) IC is derived from a 3.579545MHz crystal, using part of the MC1327P IC as an oscillator. The VDG then generates all of the signals necessary to produce a video waveform. The computer graphics information stored in the 27C128 E-PROM is accessed by the VDG to produce the desired graphics screen. In combination with the control signals from the VDG the MC1372P functions as a colour/video mixer which adds in the colour burst signal. The composite waveform is then fed to a two transistor video amplifier to produce the final output signal.

The four graphics screens contained in the E-PROM are designed using a Radio Shack colour computer and then down-loaded into the memory device. The two high-resolution screens occupy approximately 6144 bytes of memory each, and the two colour bar patterns 512 bytes each. A memory map for the E-PROM is shown in Fig.2. High res. screen 1 and colour bar 1 are located in the lower 8k of the device, whilst the other two screens are held in the upper 8k. To switch between the lower and upper areas of memory address line A13 is raised high by means of switch SW3, or by the timer/sequencer section of the circuit dependant on the position of SW4.

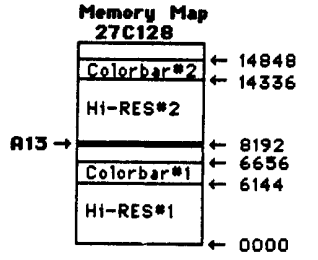


Fig.2 E-PROM Memory Map

To select the colour bar patterns the CD4066 analog switch IC is switched by the settings of SW1 and SW2, and used to disconnect the E-PROM address lines A11 and A12 from VDG control, connecting them to logic high. The VDG is also switched to the graphics mode.

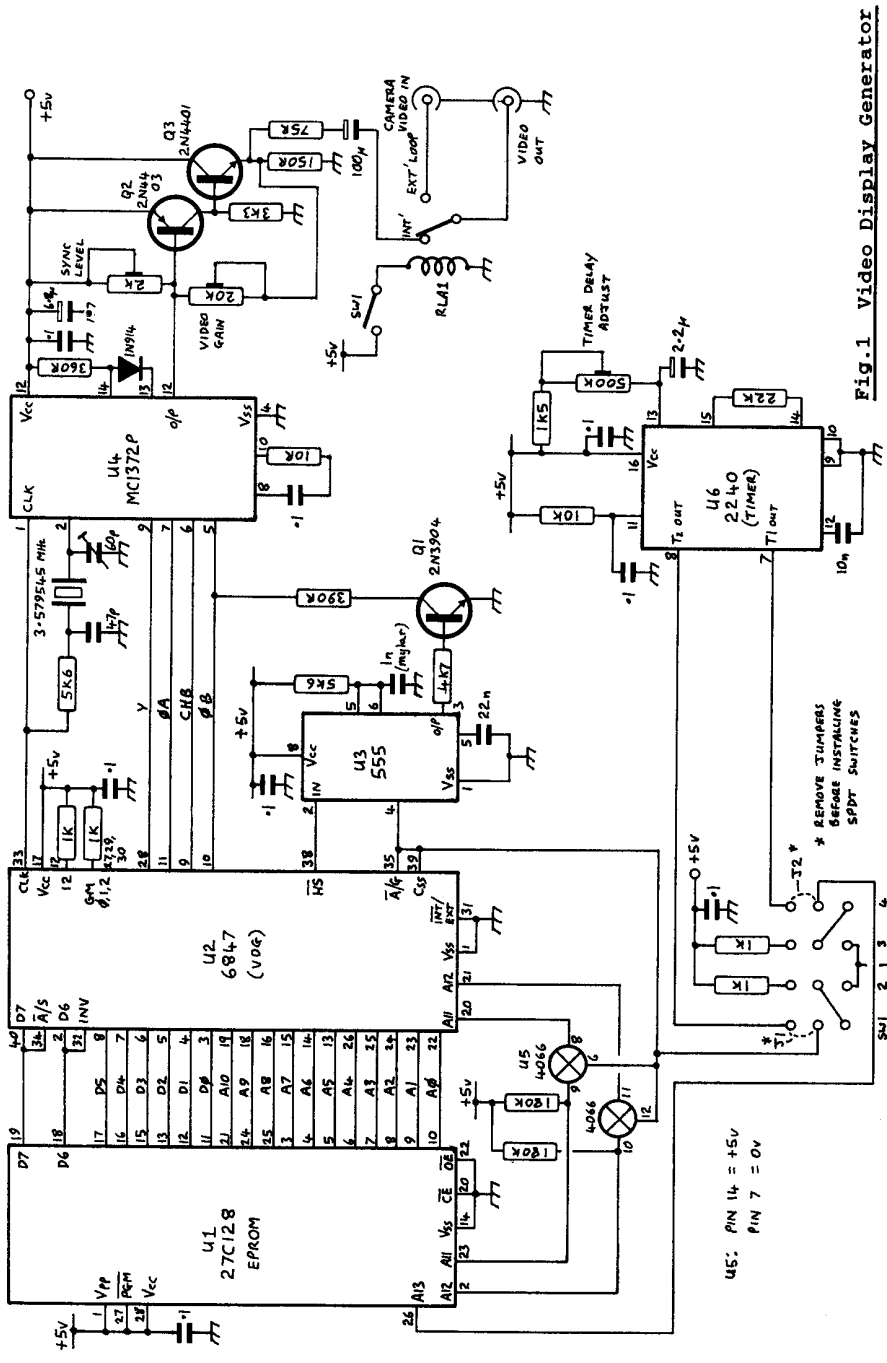


Fig.1 Video Display Generator

The VDG device is only designed to produce a black and white picture in the high-resolution mode. To overcome this a 555 Timer IC is used to generate the correct timing pulses for the MC1327P to allow a colour signal to be generated. While producing a colour video output this method does have two anomalies. Firstly, if the output is viewed on an oscilloscope it can be seen that the colour burst extends throughout the horizontal sync pulse. However, this has no effect on the video quality. The second problem is due to the fact that the VDG may start on either the rising or the falling edge of the clock pulse, thus there is a chance of getting reversed colours on the high res screens (ie: blues will be red and vice-versa). To correct this simply turn off the power supply and turn on again, repeating if necessary until the correct colours are observed. These problems only occur with the high resolution screens, correct colours are always generated in the low resolution mode used for the colour bars.

The video output waveforms of the board are shown in Fig.3. The 'white' level generated by the VDG is actually a light shade of grey, thus a ratio of 0.40 volts of sync pulse to 0.62 volts of video should be measured as shown.

The sequencer/timer function is controlled by a 2240 Timer IC. This chip is used to generate two timed outputs to control the selection of the VDG high res/colour bar mode, and the switching of the E-PROM memory banks.

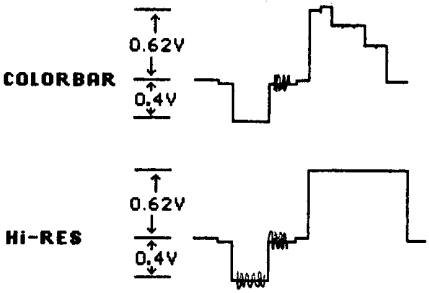


Fig.3 Video Output Waveforms

The timing of the display and its sequences are selected by the four switches SW1 to SW4. Table-1 gives the various permutations of the switches and the displays obtained. The board as supplied has links fitted at SW1 and SW4 to provide automatic sequencing through all four screens. These links must be removed before installing the switches. The switches should be wired as shown in Fig.4 so that the centre pin of the switch is connected to the centre pad of the switch PCB location. Position each switch so that when in the up position the top two pads on the PCB for that switch location are connected together, this is the ON position as referred to in table-1.

Switches SW1 and SW4 control the timer functions, SW2 and SW3 control the manual selection of the screens when SW1 and SW4 are both in the off position.

Fig.4 Switch Wiring

SW1	SW2	SW3	SW4	SCREENS SELECTED
ON	X	X	X	Sequences through all four screens.
OFF	ON	X	ON	Sequences through the two high-res screens.
OFF	OFF	X	ON	Sequences through the two colour bar screens.
ON	X	ON	OFF	Sequences through high-res 2 and colour bar 2.
ON	X	OFF	OFF	Sequences through high-res 1 and colour bar 1.
OFF	ON	ON	OFF	Manually selects high-res screen 2.
OFF	ON	OFF	OFF	Manually selects high-res screen 1.
OFF	OFF	ON	OFF	Manually selects colour bar screen 2.
OFF	OFF	OFF	OFF	Manually selects colour bar screen 1.

X = Position does not matter.

Table 1. Screen select combinations.

NOTE: For repeater applications where computer control of the graphics screens selection is desired links should be fitted between the bottom two pads of SW1 and SW4. Apply a TTL level signal (+5v) from the repeater control circuit to the centre pads of SW2 and SW3 to control the screen selection.

SETTING UP

The locations of the various connection points and potentiometers is shown on the PCB overlay in Fig,5. At the time this handbook was published the unit was only available from Bill Brown WB8ELK (address at end of article) as a pre-assembled unit. All that is required to be done is to wire up unit, the switches and other remote controls and the inputs and outputs. A suitable enclosure is the TEN-TEC JW-5. The video input and output connectors should ideally be the BNC variety. The power supply for the unit should be connected via 1nF feed-through capacitors to reduce RF interference.

Connect a monitor or oscilloscope to the output and switch the unit on. Set the VIDEO GAIN potentiometer to the 10 o'clock position and adjust the SYNC LEVEL potentiometer until a video output is present. Set up the switch positions as per table-1 to output one of the colour bar patterns. Re-adjust the SYNC LEVEL potentiometer until the yellow colour bar begins to 'white out'. The SYNC LEVEL control should be backed off until the point is reached where the yellow bar restores to normal colour. The VIDEO GAIN control is now adjusted to give the desired output level. This level may need optimising to give a correct balance between the generated screens and any through video being connected to the VIDEO INPUT, this being passed to the transmitter when the ID board is powered-down. Please note that adjustment of the VIDEO GAIN control beyond the halfway position may result in sync compression.

If external control of the timing circuit is required remove the 500k TIMER ADJUST potentiometer from the printed circuit board and install a chassis mounted type on the front panel. If longer delay times than one minute are required this potentiometer may be increased in value.

This completes the set-up procedure and the unit may now be connected into your ATV transmit system. The screens available are only limited by your imagination and Bill's (or your) computing talents.

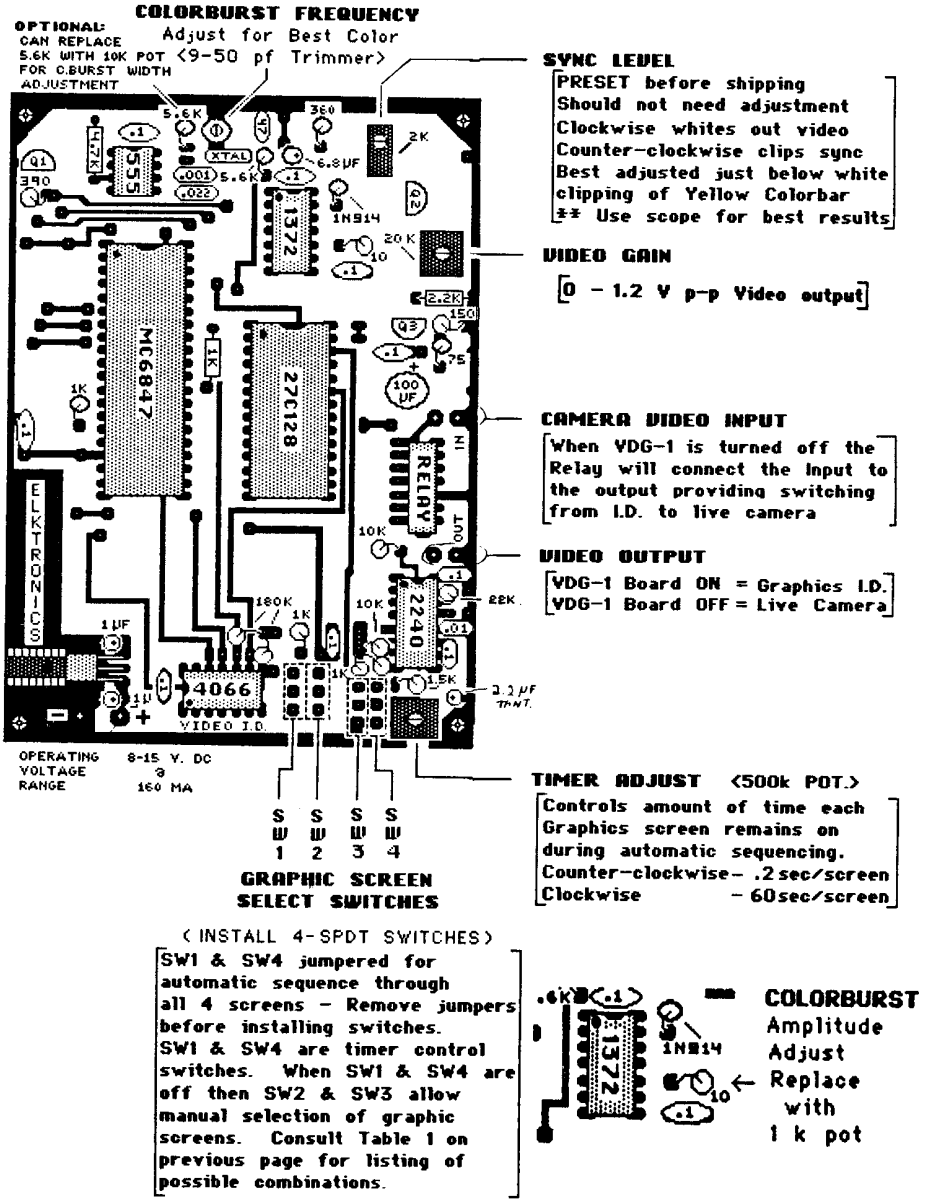


Fig.5 Component Layout

ADDITIONAL INFORMATION

If you are using a quick release E-PROM socket remember to turn off the power before changing the memory device. (This also applies even if you are using a standard socket). Ensure that the locator spot on the E-PROM is aligned correctly with the one on the socket. The E-PROM is a static-sensitive device, and as such should be stored on static-resistant foam or in a plastic storage tube when not in circuit.

For those who wish to experiment with the colour-burst circuitry the 5.6k resistor adjacent to the 555 timer can be replaced with a 10k potentiometer. This will allow the number of cycles of burst in the high-resolution mode to be varied. Also, the 10-ohm resistor adjacent to the MC1372P IC can be replaced with a 1k potentiometer in order to vary the amplitude of the burst signal. The locations of both resistor changes are shown on the inset in Fig.5.

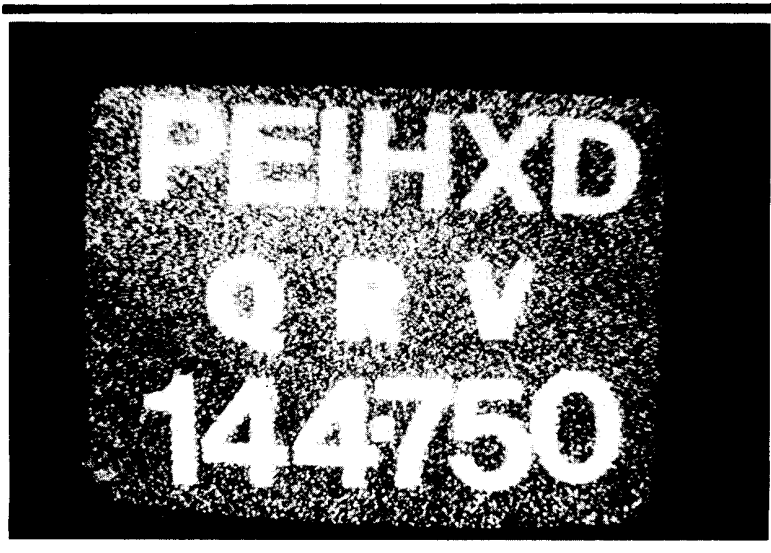
Horizontal sync pulses can be found on pin-38 of the VDG, and vertical sync on pin-37. The 3.579545MHz clock signal can be found on pin-1 of the MC1327P IC.

For further information, or to order the unit please write to:

Bill Brown WB8ELK, 12536 T.R. 77, Findlay, Ohio 45840, USA.
Tel: (419) 422-8206.

For a nominal fee Bill is also happy to layout your graphic screens from your designs and program the E-Proms with the data.

As previously stated, at the time of going to press this unit was only available pre-assembled. However, please check with Bill as to whether he is now able to supply in kit form.



TELETEXT PATTERN GENERATOR

There are plenty of circuits around for generating patterns on a television screen, and similarly there are quite a number devoted to generating alphanumeric and graphics characters. Now though, in the design presented here, both functions are made available at the same time, providing a very versatile system of electronic picture generation for the amateur shack or studio.

Teletext has been around in the U.K. for some years now under the names 'Ceefax' (BBC) and Oracle (IBA). Similar services are also available over much of Europe and many other countries throughout the world. It is not surprising then that a dedicated set of integrated circuits have been made available to satisfy the considerable demand, and it is these devices upon which this design is based. First though let's remind ourselves of the principles of the Teletext medium.

TELETEXT

The top few television lines of each television field are not used for carrying picture information as such, but for transmitter control data, specialised waveforms for checking system parameters (group delay, frequency response etc.) and other purposes. Two of the lines are also used to transmit a data system known as Teletext, whereby television sets fitted with the appropriate decoder can read this data and thus the relevant information contained in it, which comprises everything from TV programs, weather,travel, shopping etc.

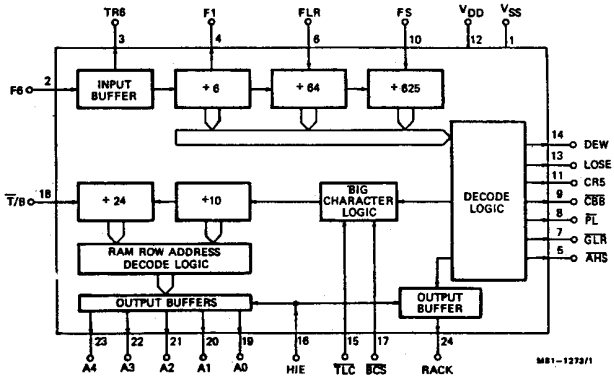
The decoder contains a 1K RAM chip which can accept a page of information at a time. All the pages are transmitted serially, but only one may be stored in the decoder at a time, once a different page number is selected by the user when it appears at the decoder the data is stored in the RAM chip. The data format is 7-bit words representing numbers from Ø to 127, each of which represents a particular ASCII character, graphic shape, colour or control code. These characters and shapes are decoded from the data stream and presented to the screen to provide the pictures and information which are read off the screen, rather like reading a newspaper. When that page has been read another can be selected and the whole process repeated.

THE TELETEXT LSI INTEGRATED CIRCUITS

SAA5020 TIC (timing chain)

The divider stages in the TIC integrated circuit sub-divide the 6MHz clock signal down to 25Hz, the television frame rate, and generate all the timing signals for the teletext display. Fig.1 shows a simplified block diagram of the SAA5020 circuits and a pin-out of the device. During the display period, a 1MHz clock signal RACK (Read Address Clock) takes over from WACK (Write Address Clock) to step the character addresses. The address counter (74LS393) is cleared at the end of every line and reset to the first position. After every ten lines during the display, the TIC steps the row address on by one to access the next row of characters in the memory.

In addition to providing all the timing signals for the display, the TIC also generates a complete composite sync signal which is used to drive the PAL coder and provide a 'stand alone' system free of any external sync requirements. The TIC is capable of genlocking to an external source but this facility has not been implemented here in order to simplify the design. Frame lock could easily be added by the reset input on pin-10 which requires a positive TTL pulse to accomplish locking. This input could be clocked at 60Hz if 525-line operation is required, not forgetting of course to adjust the frequency of the 6MHz clock to correct the line speed. The mixed sync signal is to the European standard of five broad pulses per vertical interval.



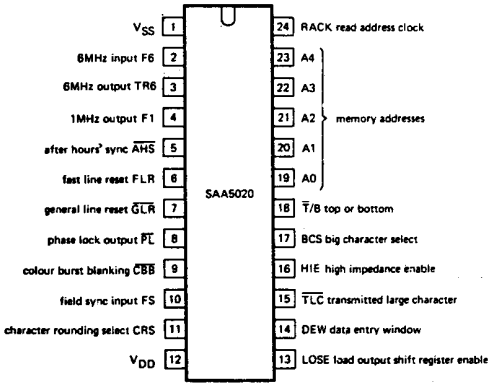


FIG.1 SAA520Ø TIC Block Diagram and Pin-Outs

SAA5050 TROM (teletext read-only memory)

The read-only memory of the TROM IC converts the 7-bit character data from the memory into a dot matrix pattern. This matrix is in a 7-by-5 dot form for each character. The TROM also contains a 'character rounding' facility which effectively increases this matrix to 14-by-10 dots, giving improved definition to the displayed characters. Fig.2 shows a simplified block diagram of the SAA5050 circuits and its pin-outs.

Timing signals are fed to the TROM from the TIC IC. Character video output signals are provided, and these comprise a monochrome-only signal (Y) and RGB signals for a colour encoder. The blanking output (not used in this application at present) enables a through television video signal to be blanked out when a teletext subtitle is to be

displayed ('1' gives 'picture blank', '0' gives 'picture on'). The blanking-out takes the form of a 'black box' around the teletext characters.

Although not used at present in this unit it is useful to describe the function of the monochrome text signal (Y). It is provided for monochrome displays; that is, it does not include background video information. However, it is also necessary if, in a normal colour display, inlay of characters into the television picture is required; it is then used as an inlay blanking signal. When text and video are mixed, the readability of the display is greatly improved if the text is inlaid, rather than simply added on to the television video. The readability is further enhanced if the picture contrast is automatically reduced when text and video are mixed.

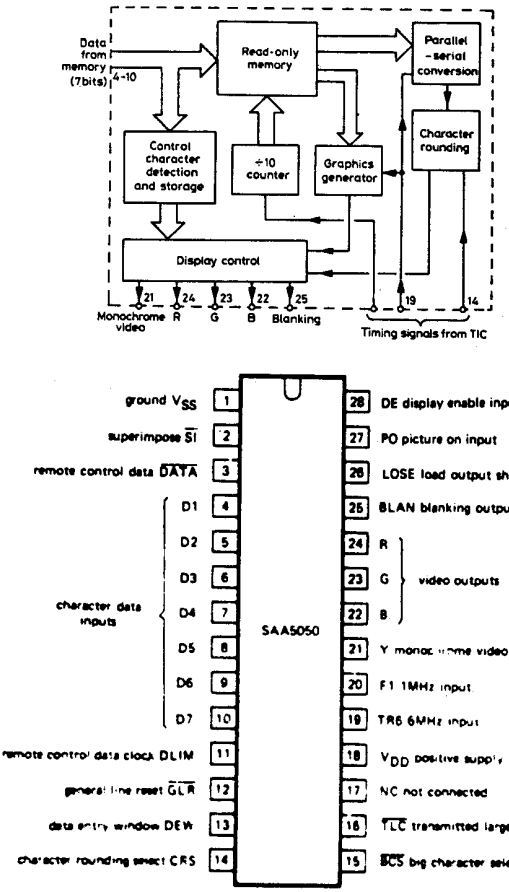


Fig.2 SAA5050 TROM Block Diagram and Pin-Outs

This can be performed by using the 'superimpose' output (pin-2) from the TROM IC.

The TROM generates 96 alpha-numeric and 64 graphics characters; the alpha-numeric character set is shown in Fig.3. In addition there are 96 special characters for controlling the display. Input to the device is a 7-bit code from the E-PROM, each character code defining a dot matrix pattern. The character period is 1uS and the character dot rate is the same as the master clock. The video output signals are all open-collector TTL signals and are at the correct amplitude for feeding the colour encoder shown elsewhere in this handbook.

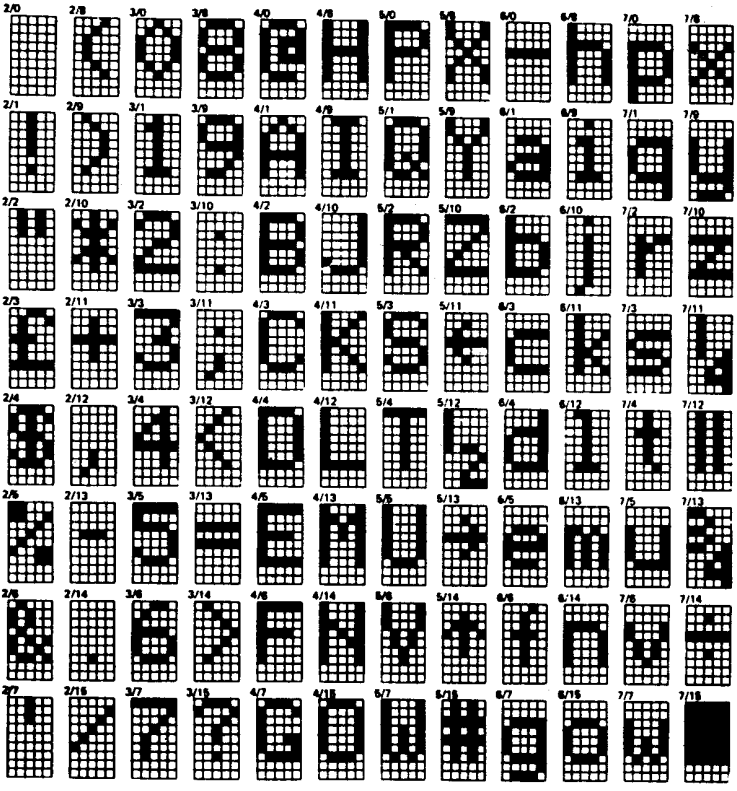
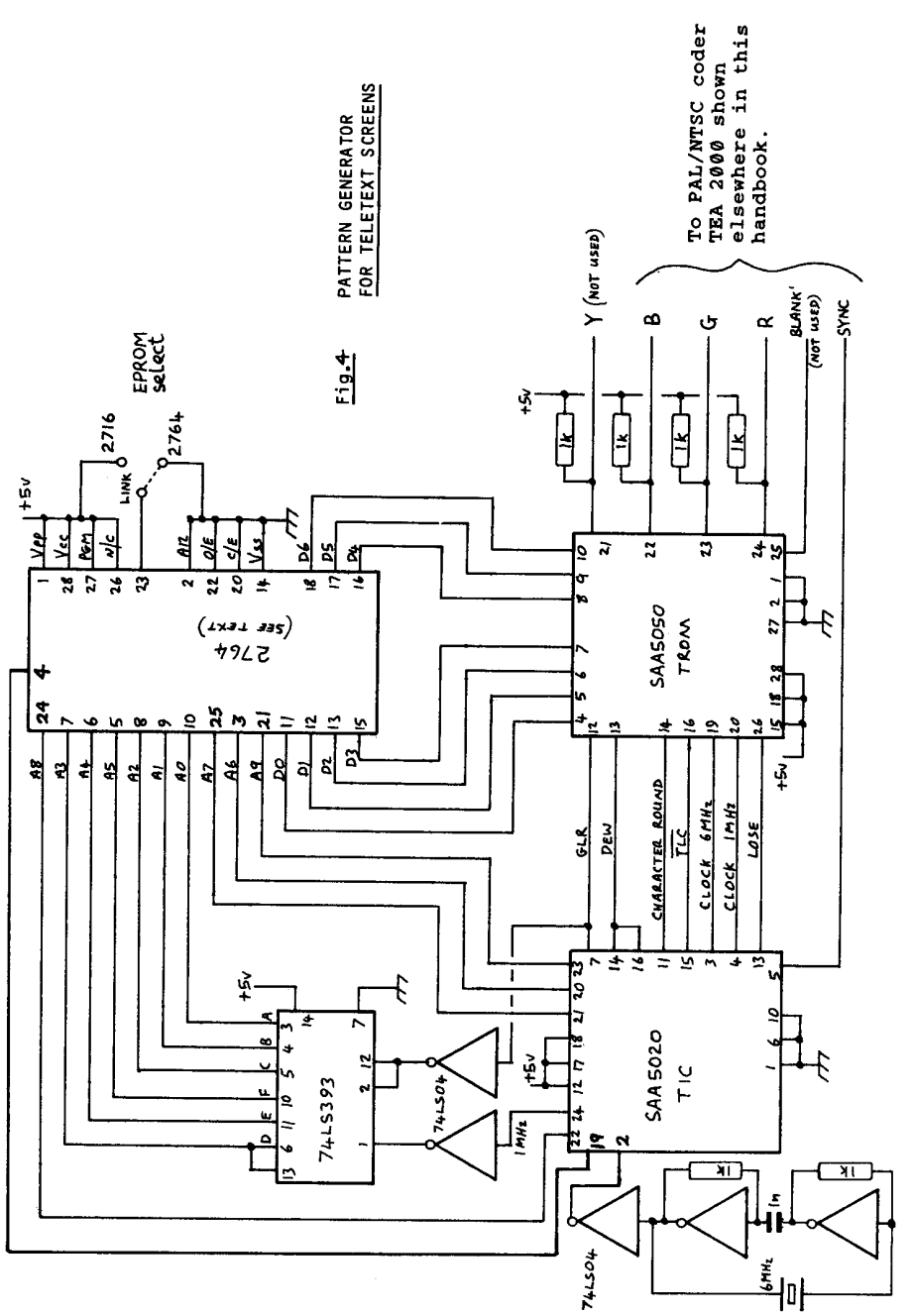


Fig.3 SAA5050 Alpha-Numeric Character Set

CIRCUIT DESCRIPTION

The circuit diagram is shown in Fig.4. The 6MHz system clock is generated by two gates of a 74LS04 Hex Inverter and is controlled by a 6MHz crystal. This clock is used to derive all the necessary timing edges for all the waveforms. The 24-pin SAA5020 Timing Chain IC generates the mixed sync, colour burst and, with the aid of the 74LS393 Counter, all the memory addresses for reading the E-Prom. This IC is capable of genlocking so that the video display is synchronous with an external source, but this has not been implemented here in order to simplify the circuit. Frame lock could easily be added by the reset input on pin-10 of device, which requires a positive TTL pulse to accomplish this task. This input could also be clocked at 60Hz for 525-line working as well as adjusting the frequency of the 6MHz clock to correct the line speed. The mixed sync is to the European standard of five broad pulses per vertical interval.


PATTERN GENERATOR
FOR TELETEXT SCREENS
Fig.4
To PAL/NTSC coder
TBA 2000 shown
elsewhere in this
handbook.
EPROM
select
2716
2764
LINK
+5v
2764A
(SEE TEXT)
SAA5050
TRDM
SAA5020
TIC
74LS393
74LS04
74LS04
1MHz
6MHz
Y (NOT USED)
B
G
R
BLANK
(NOT USED)
SYNC
GLR
DEW
CHARACTER ROUND
TLC
CLOCK 6MHz
CLOCK 1MHz
LOSE
1k
1n

The SAA5050 Teletext Character Generator IC is a 28-pin device which incorporates a fast access character generator ROM (4.3K) and the decoding circuitry for all the teletext control characters. The device generates 96 alpha-numeric and 64 graphic characters. In addition there are 96 special characters for controlling the display. The input to the device is a 7-bit code from the E-Prom, each character code defining a dot matrix pattern. The character period is 1uS and the character dot rate is the same as the master clock, ie:6MHz. The video outputs from the device comprise a monochrome output (Y output, not used here), and Red, Green and Blue. These outputs are all open collector TTL signals and are at the correct level for feeding, along with the mixed sync, the colour coder shown elsewhere in this handbook.

The RAM memory used in television teletext decoders has been replaced here by the E-Prom, which may be either a 2716 or 2764 type. If a 2716 is used it should be located at the bottom of the socket leaving the top four pins (two each side) vacant, and the link at pin-23 changed to the +5v position. A pre-programmed E-Prom can be obtained from BATC Members Services with the pattern shown in Fig.3. Alternatively, for those able to program their own devices Fig.4 shows the area of the memory which is addressed by the circuit. For those owning Spectrum computers an E-Prom Blower is described elsewhere in this book.

CHARACTER MAPPING AND FORMAT

The screen memory map is peculiar to this circuit. The format is 40 characters across the screen stored in 64 bytes of memory, the remaining 24 bytes being skipped over and the next line of information starting at memory location 65 (see Fig.5).

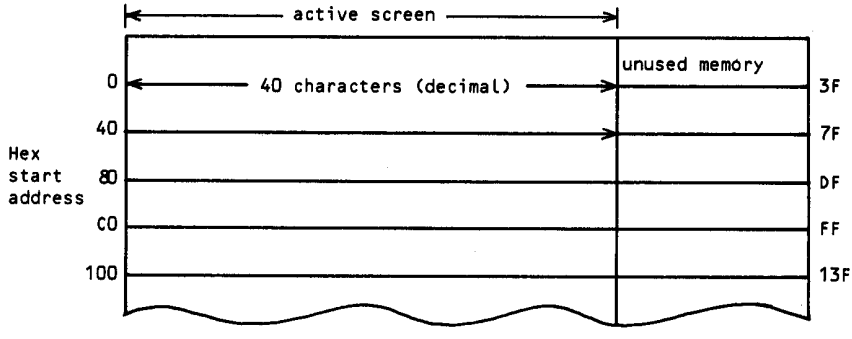


Fig.5 Screen Memory Map

Each character occupies a space six dots wide by ten lines high, (Fig.6) one dot space is left between adjacent characters and one television line space left between rows. Alpha-numeric characters are generated on a 5x9 matrix thus allowing space for true descenders. Each of the 64 graphic characters is decoded to form a 2x3 block arrangement which occupies the complete 6x10 dot matrix.

The alpha-numeric characters are rounded, that is a half dot is inserted before or after a whole dot in the presence of a diagonal in a character matrix. Graphic characters may be either contiguous or separated (Fig.7). The control characters allow the nature of the display to be changed, eg: double height, character colour, flashing display, background colour etc.

The table in Fig.8 shows the complete character and control code set and gives the HEX code for each. The selection between alpha-numeric or graphic character for each HEX code is carried out by first selecting or cancelling the graphic mode, using the appropriate code for that instruction.
This is exactly the same method as is used in home computers.

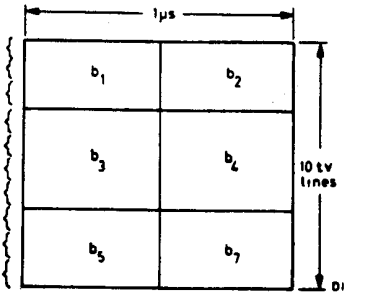
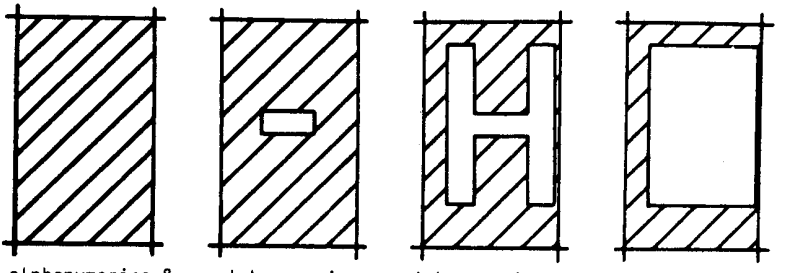


Fig.6 Character Cell



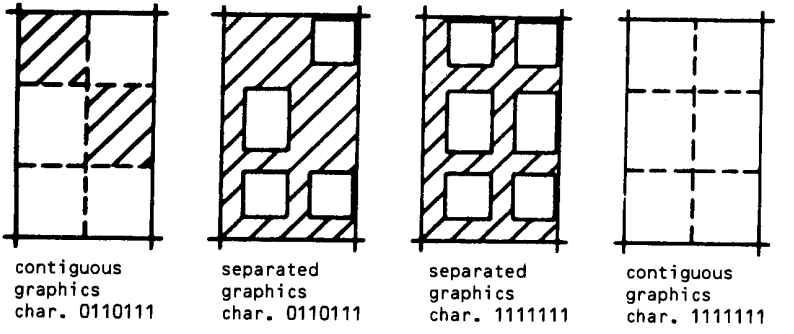
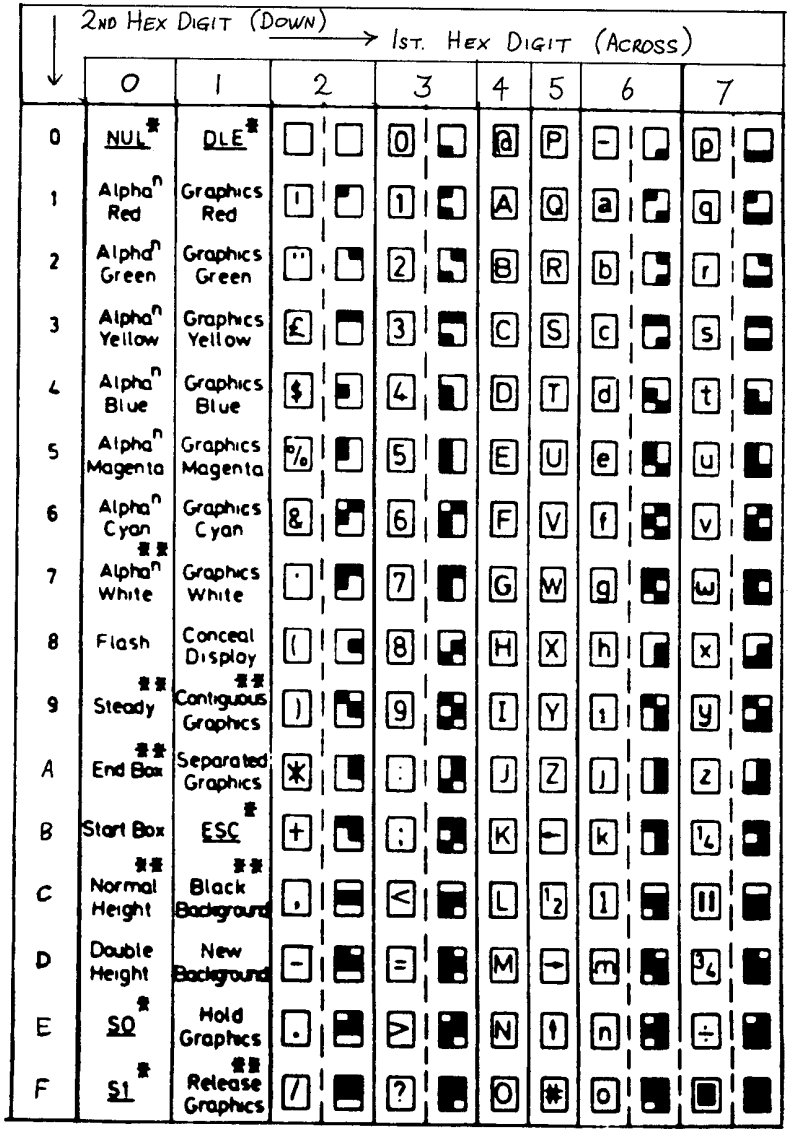


Fig.7 Graphic Character Make Up



EG: HEX CODE FOR 'A' = 41

Fig.8 Hex Codes for Character Set

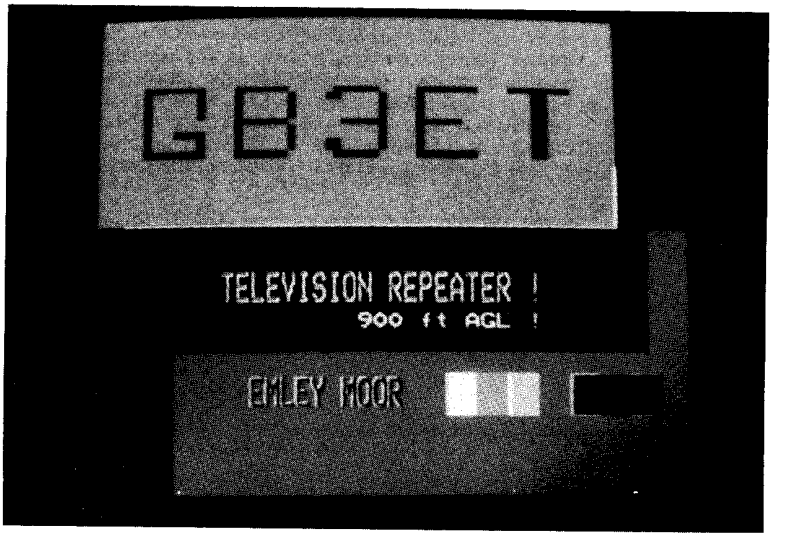
CONSTRUCTION

A pre-drilled printed circuit board for this unit is available from BATC Members' Services. The PCB will accomodate either HC6U or miniature crystal packages. It is recommended that all the IC's are mounted in sockets, and as the circuit board is single-sided this will not cause any problems. The E-Prom can be a 2716, 2732 or a 2764 type. Pin-23 is left floating on the PCB, thus a solder bridge is all that is required to suit the appropriate device. The 2716 and 2732 types are housed in 24 pin packages and should be fitted into the socket so that the unused holes (socket locations 1, 2, 27 & 28) are at the top.

As previously stated, the RGB and sync outputs are at TTL, and suitable for feeding directly into the PAL/NTSC coder shown elsewhere in this handbook.

A selection of pre-programmed E-PROM's is available from Members's Services, but only with the patterns shown customised with your own call sign, QTH etc.

The chip set which decodes the data and display can often be found on the surplus market at very reasonable prices. Alternatively, they are regularly advertised in the national magazines by the large electronic spares retailers.



An example of a screen produced by the Teletext pattern generator.

DUAL-STANDARD COLOUR CODER

Several of the projects in this handbook require the addition of a colour coder to provide a suitable video output waveform for use in the shack. Although this simple coder could be added on to the PCB's for each unit, it has been designed as an add on to allow it to be used with other units not described in this book. The coder is suitable for both PAL and NTSC standards and is easily configured for either.

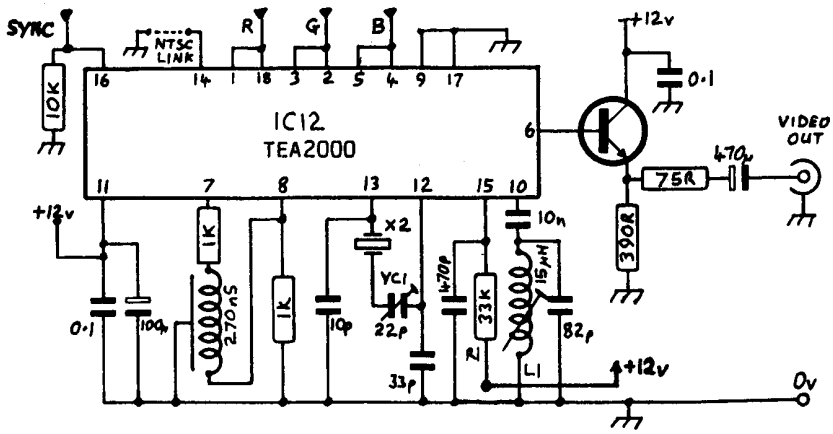
CIRCUIT DESCRIPTION

The colour coder is contained within a single chip the TEA2000. This device is capable of encoding to NTSC or PAL standards by either grounding pin-14 for NTSC, or leaving it 'floating' for PAL. The crystal connected to pin-13 (x2) needs to be twice the frequency of the colour subcarrier, ie:8.867MHz for PAL and 7.1276MHz for NTSC. L1 should be adjusted for maximum subcarrier and the burst position may need altering between standards, this is done by changing the value of R1. The delay line at pin-8 should be a 270nS type (Philips V8470 270nS/900-ohm), as found in domestic TV sets.

CONSTRUCTION AND SET-UP

A printed circuit board is available from Members' Services for this project. The TEA2000 and the delay line may also be available, please check your latest copy of CQ-TV.

Once all the components have been fitted and soldered to the pcb connect the input signals, the DC supply and a colour monitor to the output. Set the solder link at pin-14 of the TEA2000 to either floating for PAL, or to ground for NTSC (also check that the correct frequency crystal is fitted for the standard in use as given above). Adjust VC1 until colour-lock is obtained, confirming that the trimmer is in the centre of the lock-in range. Adjust L1 for maximum colour saturation.



VIDEO DISTRIBUTION AMPLIFIER

A problem often encountered in the shack is the need to supply several different pieces of equipment from the same video source. What's required is a simple, but effective, video distribution amplifier. The unit described here fulfils that requirement, in fact it is so simple it almost belies description. It will provide three outputs from one input.

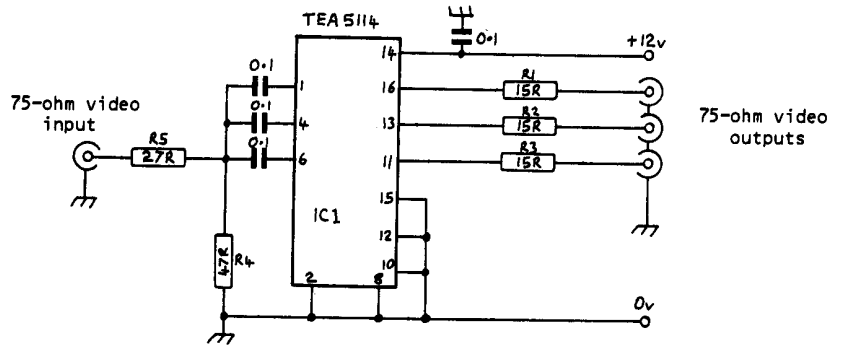
CIRCUIT DESCRIPTION

The heart of the unit is the video switching IC the TEA5114. In this circuit this chip is not used for its switching capabilities, but for its signal amplification and isolation properties. The input video signal is fed to each of the normally closed inputs of the device via separate decoupling capacitors. The three outputs are taken via 15-ohm resistors, maintaining the impedance at 75-ohms.

The switching control inputs of the TEA5114 (pins-10, 12 & 15) are all grounded, thus preventing operation of the switches. However, if it is required to be able to switch off the various outputs, then by applying a MAXIMUM of +2.5 volts to the appropiate control input, the respective output will be switched off.

CONSTRUCTION

This unit being so simple can be constructed in a very short time using Vero-board, thus a printed circuit board has not been made available. No special attention needs to be paid to the layout of the few components. A single 12 volt power rail is required capable of providing 150mA.



Video Distribution Amplifier

A DIGITAL FRAMESTORE

This project is fairly complex and ideally should not be attempted by the inexperienced constructor

The television signal that is handled by most of our television equipment consists of an analogue part (the picture content) and a digital part (the timing or sync. pulses). The analogue part has continuous variations of amplitude and is easily affected by distortion or interference.

In transmitting signals Frequency Modulation is capable of higher quality, once a threshold is reached. The amplitude of the received signal does not matter and most interference etc is, essentially, sliced off by the processing of the signal in the receiver. In a similar way digital audio, from tape or compact disc, is capable of high quality if suitably processed. If, therefore, the analogue part of a video signal can be turned to a digital signal we can process it in various ways, without causing distortion. In video, in fact, it is the ability to process the signal which is the greatest benefit.

In order to make use of digital video signals, a number of decisions need to be made as to how the video is to be processed. For example, the video may be digitised in composite or component form, the signal may be sampled at various rates, and so on. In this project many of these options are left open, in order to make it adaptable to future expansion or different television standards. For colour working, however, the picture signals will be treated in component form - which will enable standards conversion, for example, if that is later required. The project is designed in a modular form, for ease of testing and to allow for improvements to a section without making the remainder redundant.

The essentials of a digital video system are shown in the block diagram (Fig 1). The video input has first to be sampled at an appropriate rate. Thus a clock pulse locked to the incoming signal will be needed for this. The resultant digital video is then processed, which may include storing in memory. For this an address will need to be determined for each point of the picture to be written into the RAM. To read out the signal a series of read addresses will need to be sent to the memory, and the signal may be further processed. The outgoing digital signal will then need to be converted back into a conventional video signal, which will need a clock pulse locked to the read addresses. These various circuits are accomodated on a series of Eurocard printed circuit boards available from Member's Services, which can be added to as the system develops.

ANALOGUE TO DIGITAL TO ANALOGUE CONVERTER

This first board contains the circuits to carry out the conversion from analogue video to digital signals, generate the incoming locked clock pulses, and convert the digital signals back to an analogue video signal. The circuit is shown in Fig 2 and works as follows: The incoming video signal is terminated by the 75 ohm resistor, then amplified by the LM318. This has a capacitor across the feedback resistor (4p7 in the diagram) to provide some high frequency roll-off to the response, and reduce the patterning that can result from beats

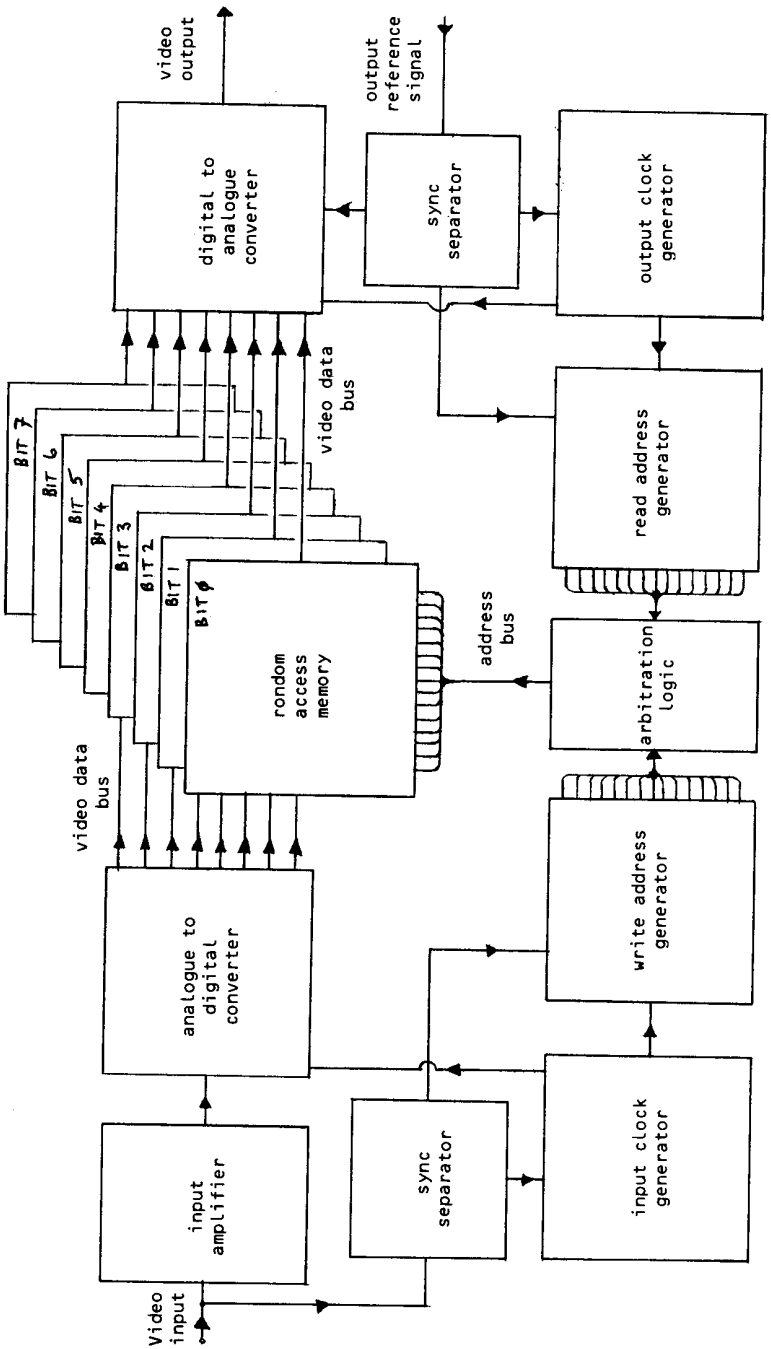


Fig.1 FRAME STORE BLOCK DIAGRAM

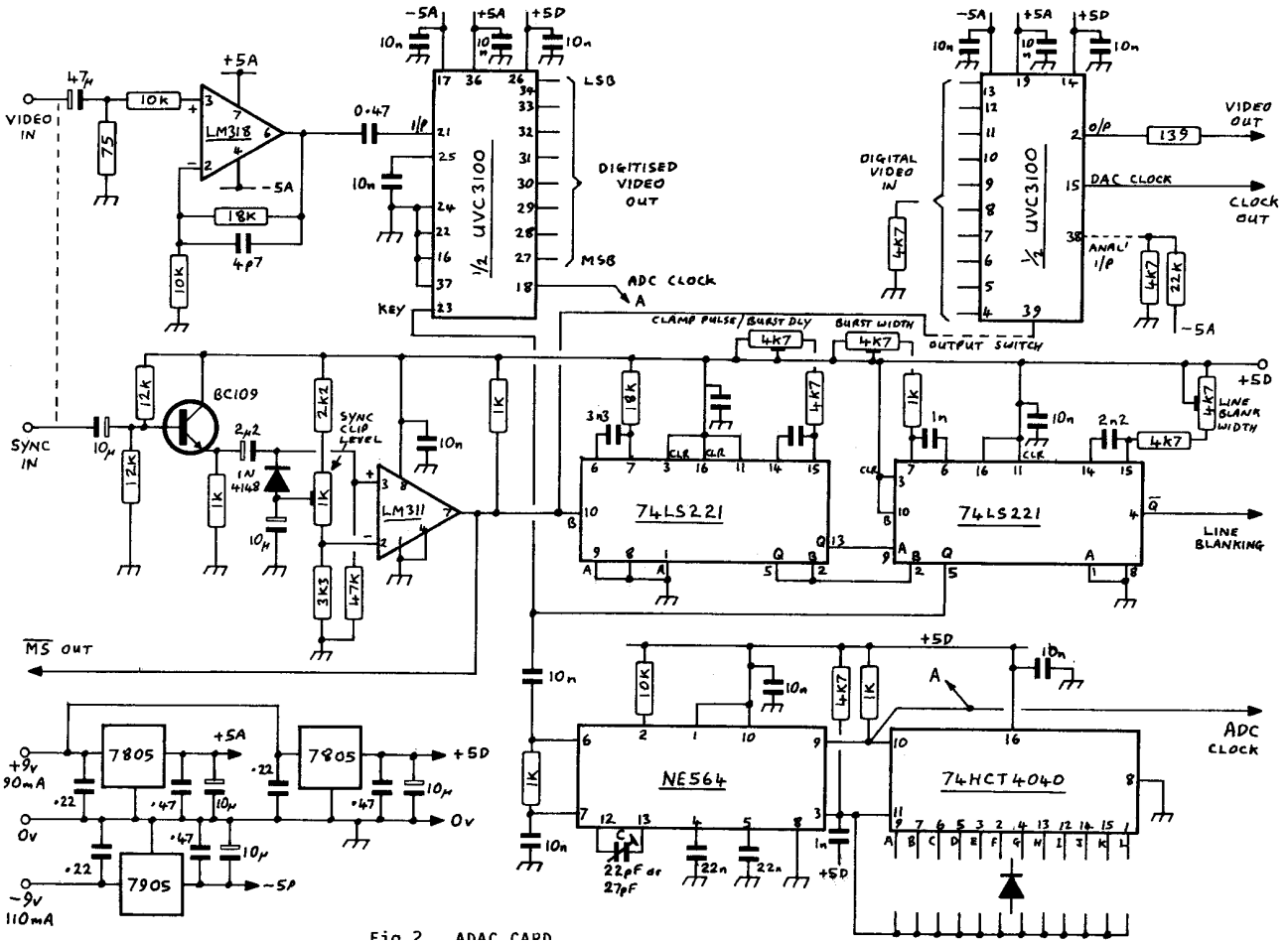
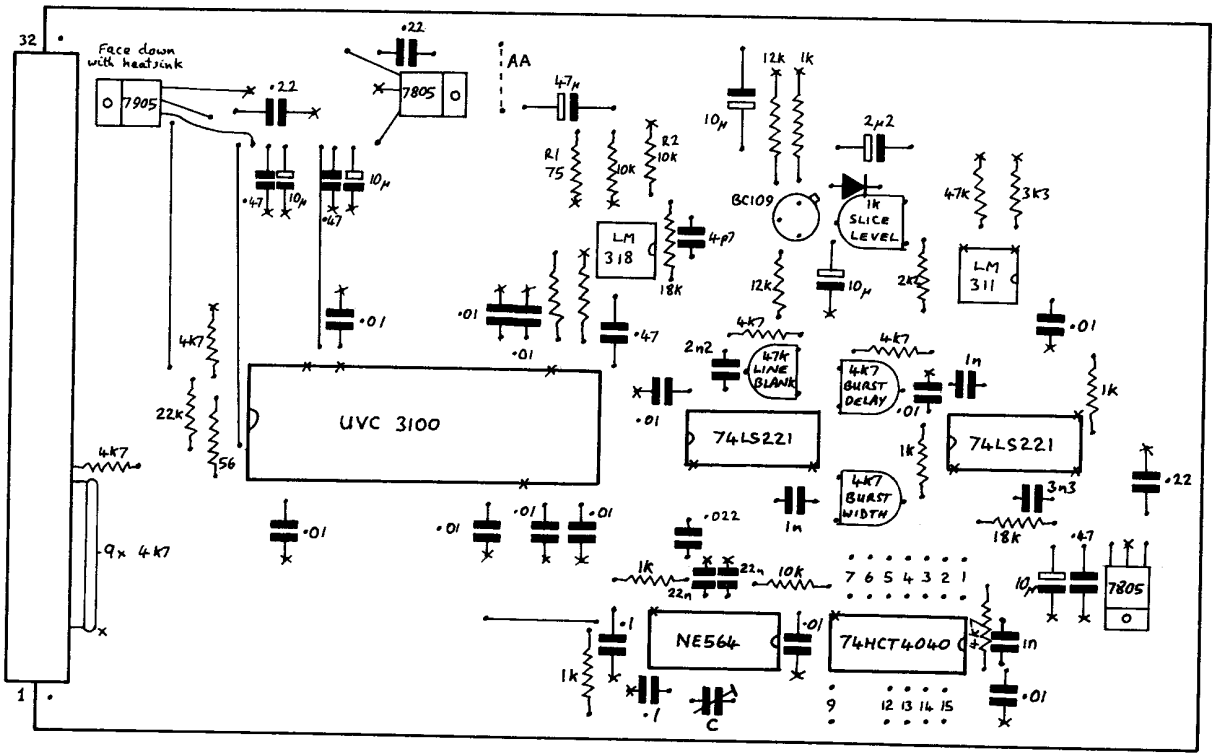


Fig 2 ADAC CARD

Fig.2 ADAC CARD



x = connection to ground plane

Pin connections

32	MS in	
31	+5v supply	
30	$\overline{\text{MS}}$ out	
29	-5v supply	
28	video input	
27	L BL out	
26	BG out	
25	MSB	ADC out
24		
23		
22		
21		
20		
19		
18	LSB	
17	ground	
16	o/p switch p39	
15	ext i/p pin 38	
14	output	
13	ground	
12	MSB	DAC in
11		
10		
9		
8		
7		
6		
5		
4		
3	LSB	
2	DAC clock	
1	ADC clock	

Fig.3 A-D/D-A PC BOARD LAYOUT

between the clock pulses and high frequencies in the video signal. Increasing this capacitor will reduce the video bandwidth of this amplifier, and vice versa. The video is then fed to the UVC3100, which clamps the video signal to black level, and then carries out an A-D conversion. The video is sliced into 256 possible grey levels, and coded into an 8 bit binary word, for each sampling point.

A sync signal is either taken from the incoming video or as a separate feed, buffered by the BC109, and fed to the LM311 comparator circuit which slices the sync pulses off. The output is therefore inverted mixed sync pulses. These are fed to a 74LS221 monostable, which removes the half line pulses, and triggers two further monostables - one producing a pulse that lasts until the end of line blanking (required by the write address circuit) the other producing a delay to trigger the fourth monostable to generate a clamp pulse for the UVC3100 input clamp. This can conveniently be set to coincide with the colour burst. This signal also triggers the phase comparator of the phase lock loop that generates the incoming video clock pulses, which is made by the NE564 and 74HCT4040. It can be adapted to run at almost any desired clock rate by choosing a suitable value for the capacitor C at NE564 pins 12 and 13 and by changing the programming diodes of the 74HCT4040.

The clock pulse is not locked to the subcarrier frequency, so that if the picture is to be rescaled, or in some other way distorted spacially, the colour can still be handled. This will require the colour to be handled in component, not composite form.

Also on this board, because it is contained in the UVC3100 I.C., is the D-A converter. This takes in a 10bit digital signal - of which the 8 most significant bits can be used at this point (pins 4 - 11 in order) - and converts it. There is also an analogue switch at the output which can be used to insert clean sync pulses etc. The card will also accept on board voltage regulators, which together with decoupling at the supply pin of each I.C. will prevent noise problems.

This board can be made tested and used on its own and the layout is shown in Fig 3. The 7805 regulators use the ground plane directly as the heatsink, whilst the 7905 must be insulated from the copper bracket which transfers its heat to the ground plane.

The oscillator frequency is now decided. For those who wish to decide this themselves, the method is given below - others can move on to the next paragraph! The UVC3100 can handle a sampling frequency up to about 30MHz, but a much lower frequency is quite acceptable for video. If the data is to be stored in memory then this may decide the maximum. For example, a 256k RAM has 262144 locations. The active part of a 625 line picture is contained in 288 lines per field, so if the memory were filled up then there would be 910 (262144 / 288) samples per line. These occupy the active part of a television line (52 micro seconds at 625 lines) so across the full line (64 micro seconds at 625 lines) there are 1120 samples (910 x 64 / 52). Each sample takes 64 / 1120 micro seconds - which is 57.14 nS, corresponding to a frequency of exactly 17.5MHz. To set the NE564 frequency, we need a capacitor C where:

C = 400 / f ('C' is measured in pF, 'f' clock frequency in MHz). This comes out at 22.8pF in the example so a 22pF trimmer capacitor is

fitted. Diodes are inserted in the positions that, from Table-1, add up to the number of samples per total line (1120) in order to program the 74HCT4040 divider. In the example this is F, G and K (32 + 64 + 1024) - there is only one possible combination for any particular clock rate. By following the method above, any desired clock rate can be accomodated on this board for any television standard.

DIODE LOCATIONS	A	B	C	D	E	F	G	H	I	J	K	L
NUMBER OF SAMPLES	1	2	4	8	16	32	64	128	256	512	1024	2048

TABLE-1

Using diodes at F, G, I and J, (Fig's.3, 8 and 9 locations 2, 4, 12 and 14) together with a 27pF trimmer capacitor gives a 13.5MHz clock rate, whilst diodes at F, G and K (Fig's.3, 8 and 9 locations 2, 14 and 15) with a 22pF trimmer capacitor give a 17.5MHz clock (both for 625 line / 50 field pictures).

SETTING UP THE ANALOGUE BOARD

Now apply a 1 volt p-p video signal to the input. Monitor the signals at the LM311 pins 2 and 3 with a D.C coupled oscilloscope, and adjust the slice preset potentiometer, so that the slicing point is about half the sync pulse amplitude. The oscilloscope is now used to adjust the three other presets - putting the incoming video on one channel and setting the end of blanking to coincide with the start of the incoming video. Also set the clamp pulse to be between the sync pulse and start of active part of line (i.e., where the colour burst would be) this is quite easy.

Trimmer capacitor C at the NE564 is adjusted as follows: Monitor the signal on pin-6 of the NE564 on channel-1 of a twin beam oscilloscope, connect channel-2 to pin-6 of the NE564. Trigger the oscilloscope from channel-1 and adjust trimmer C until the signal on channel-2 is locked to channel-1

Lastly, switch off, couple the digital output lines in order to the eight most significant digital input lines, and connect the two clock lines together. Apply the video signal to the board input, and a reconstructed copy should be seen at the DAC output. Looking at it on the oscilloscope, it will appear to be displaced about 150 - 200nS to the right (i.e. 3 clock pulses), the time taken for all the processing.

This circuitry has been designed and tested using the UVC3100 analogue-to-digital interface circuit. It is one of several similar circuits which may be used with minor circuit changes. The UVC3101 is pin for pin matched to the '3100 device, but has a slightly less linear D-A converter. The UVC3120 lacks the input clamp, buffer and voltage reference circuitry. Pin-25 must be held at +2V, and pins-20, 22 and 23 grounded if this circuit is used. The UVC3130 is virtually the same as the '3100, but requires +5V analogue supply to pins-1 and 40 (which are unused pins in the other versions).

As it stands the board can be used to change the number of grey levels

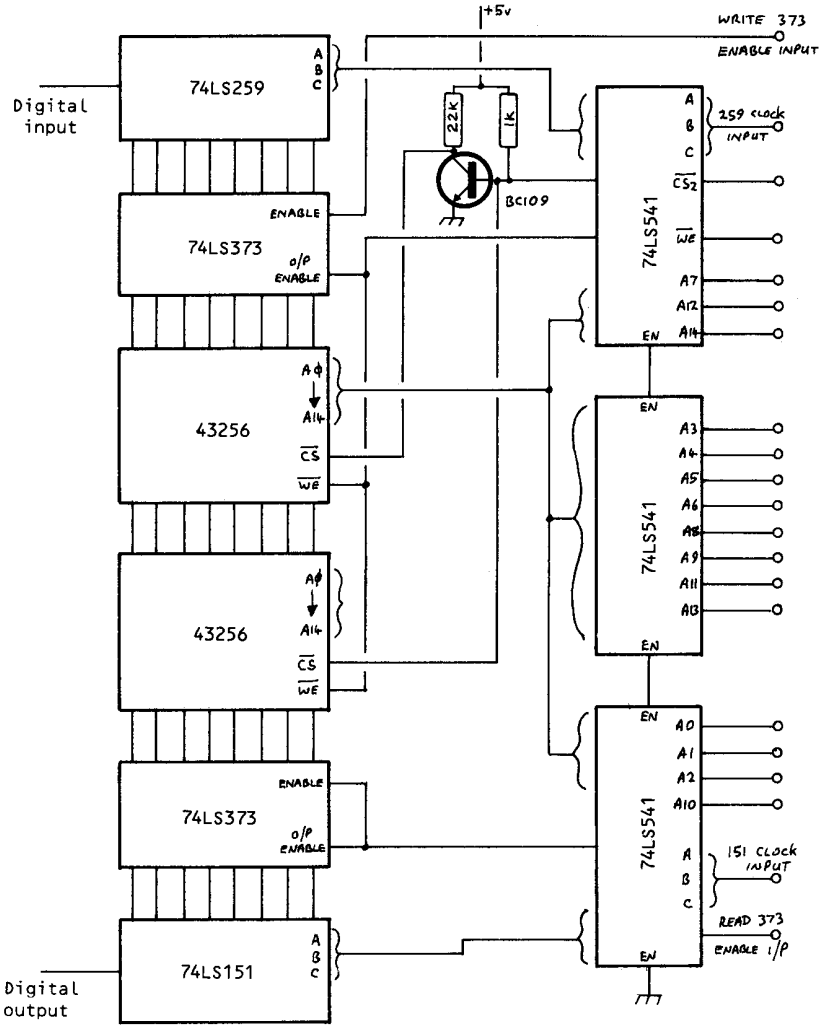
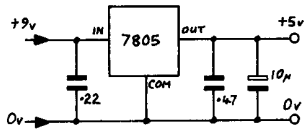


Fig.4 RAM CARD



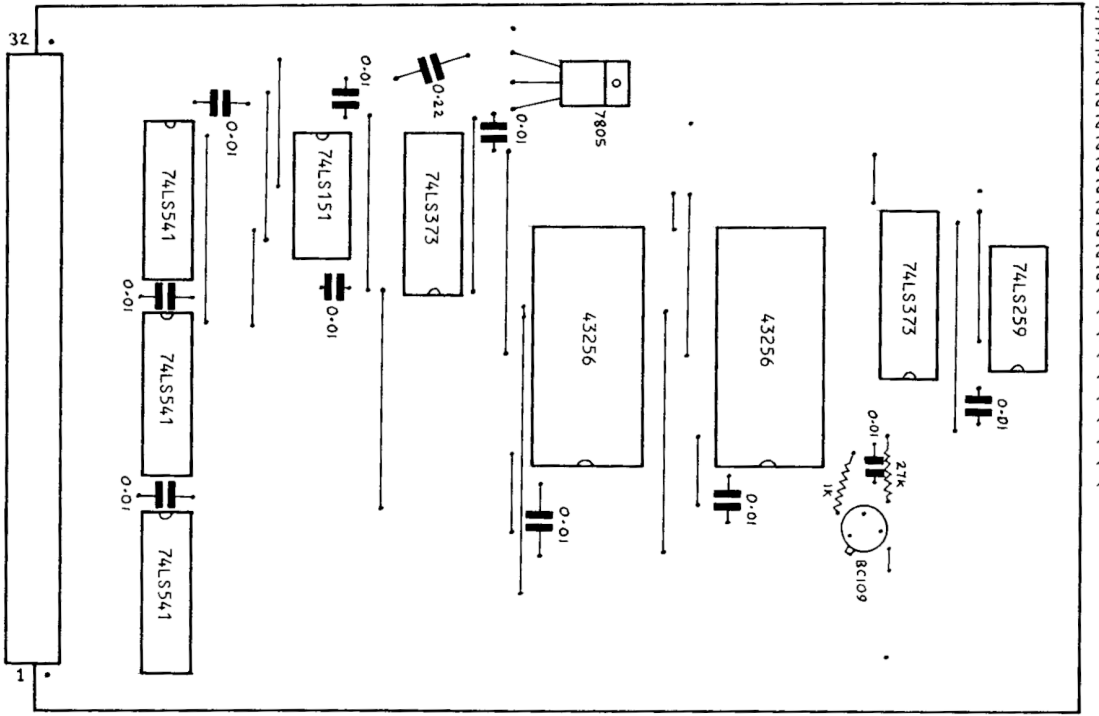


Fig.5 BATC RAM CARD

Pin Connections

32	
31	input enable '373 pin 11
30	+ve supply
29	output
28	input enable '259 pin 14
27	output tristate '373
26	C
25	B } '151 clock output
24	A
23	A0
22	A1
21	A10
20	A2
19	ground
18	A3
17	A11
16	A4
15	A9
14	A5
13	A8
12	A6
11	A13
10	A7
9	A12
8	A14
7	read/write control
6	CS2
5	A
4	B } '259 clock input
3	C
2	input
1	CS1

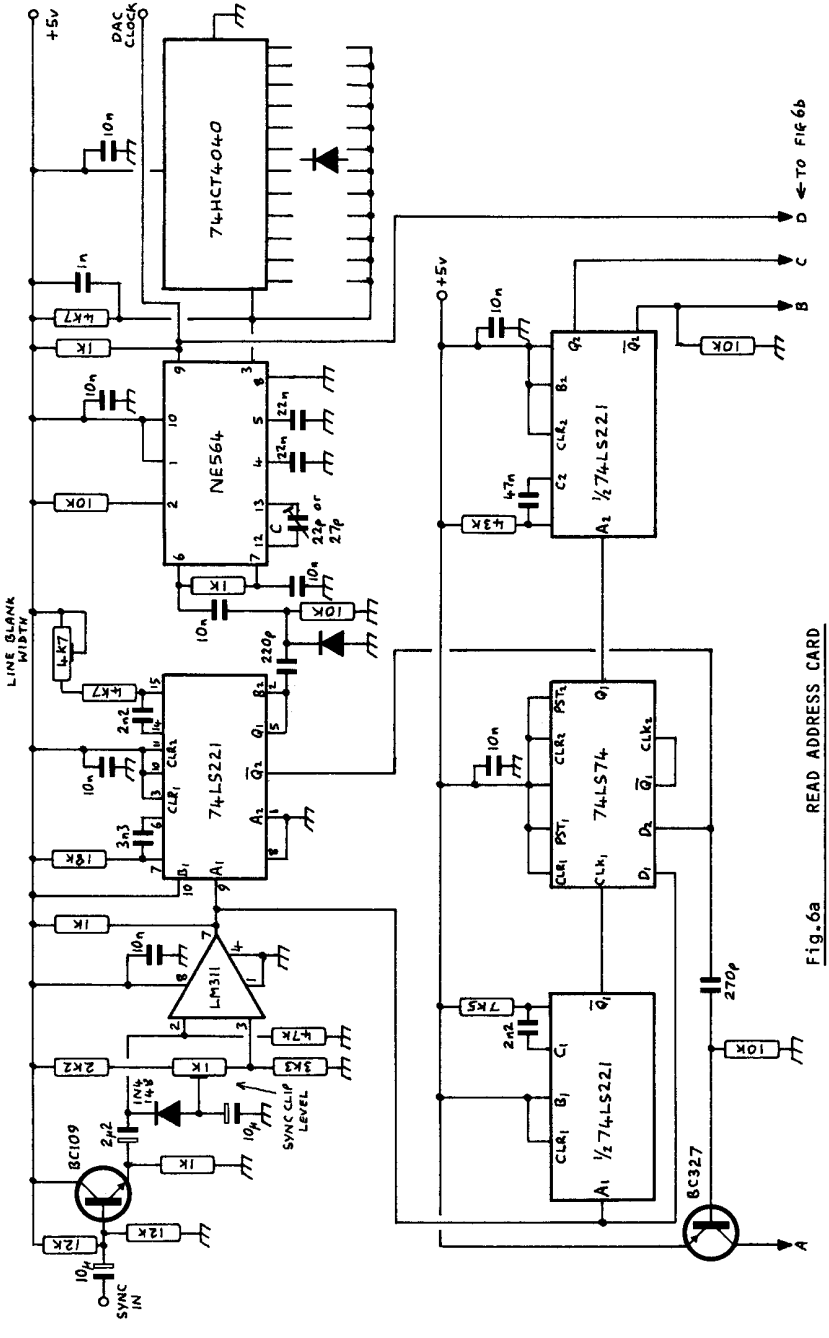

+5v
DAC CLOCK
74HCT4040
NE564
74LS221
LM311
BC109
BC327
SYNC IN
SYNC CLIP LEVEL
LINE BLANK WIDTH
74LS74
½74LS221
TO FIG 6b
READ ADDRESS CARD

Fig.6a

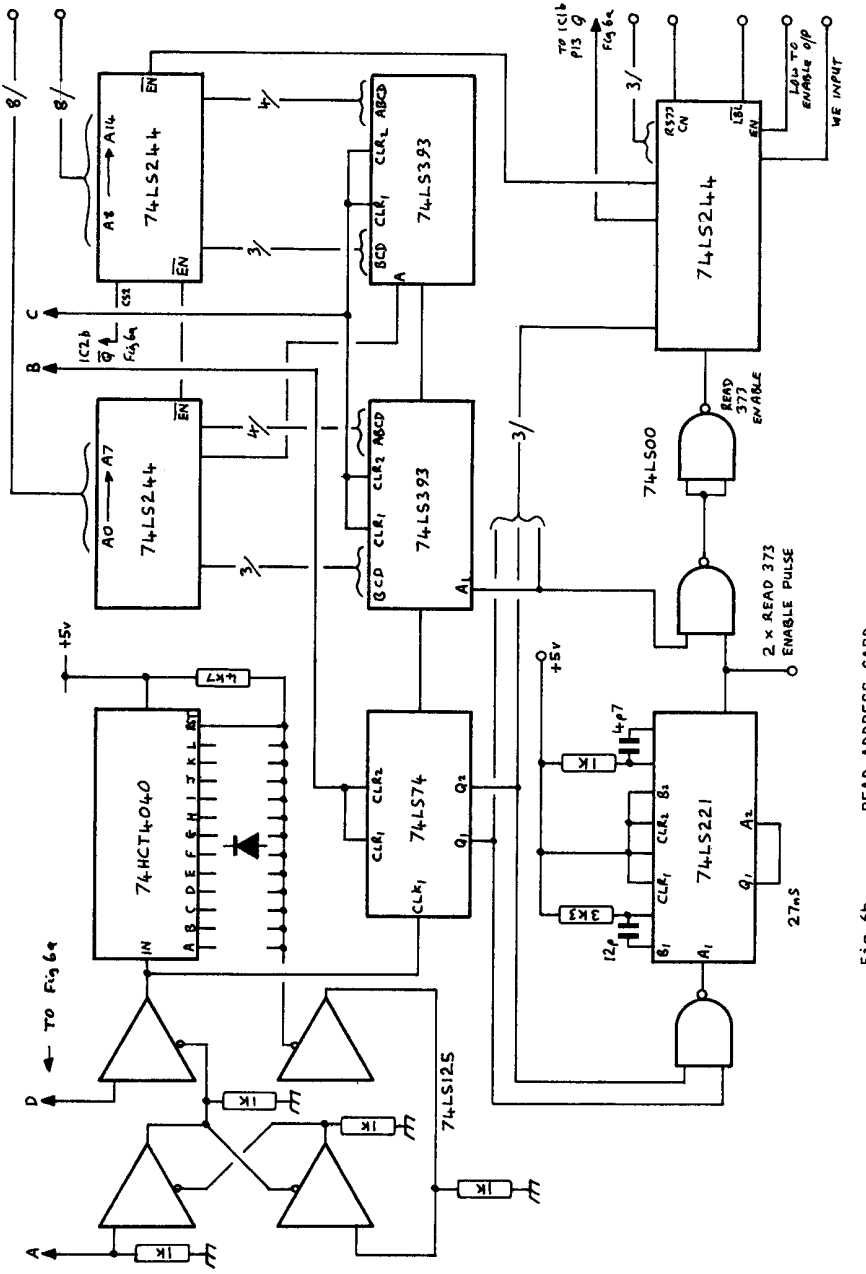

74LS244
74LS393
74HCT4040
74LS74
74LS221
74LS125
74LS00
+5v
1K
4K7
4µ7
3K3
12p
27nS
TO Fig 6a
TO IC1b pin 9 Fig 6a
2 × READ 373 ENABLE PULSE
READ 373 ENABLE
WE INPUT
READ ADDRESS CARD

Fig.6b

in the picture. By putting switches in the digital path, or by inverting the digital signals, negative images can be selected. However, if the digital data is stored in memory a much wider range of applications become possible.

NOTES: 1) If the input is not required to be terminated in 75-ohms, remove the 75-ohm resistor connected to ground at the junction of the 47uF input capacitor and the 10k resistor.

2) Replace the 10k resistor to ground connected to pin-2 of the LM318 with a 22k for composite colour signals.

3) Insert link A-A to enable sync extraction from the incoming signal.

RAM AND READ/WRITE ADDRESS CARDS

To put the data into RAM is not quite staightforward. Even at the 'slow' speed of 13.5MHz, a new sample comes along every 74nS or so - at 17.5MHz this happens every 57nS. The data has to be read into the memory and also a (probably different) sample read out sufficiently quickly to allow the next sample to be read in. At first this may appear to be impossible, or to at least need RAM with an access time of less than 28nS. The trick is to allow the A-D converter to send data every 74nS, but only ask the memory to accept data every 592nS. Using readily available 120nS access time RAM devices there is now plenty of time to do this, and read out a sample every 592nS as well. It would appear that seven out of eight samples will be lost as a result, but they are stored temporarily, and eight parallel bits of data read to the main RAM every 592nS. In many designs the temporary storage is done in shift registers, but here (Fig 4) the addressable latch (74LS259) does the task. Once the 8 latches are full, the data is held in latches (74LS373) until the RAM is ready to accept it. In a similar way, the data is read out of the RAM as eight parallel bits of data, held temporarily in a latch (74LS373 again) and returned as a serial stream of digital video by the data selector (74LS151). Static RAM is used, as this greatly simplifies the addressing requirements, which will be an advantage if extra facilities are added later. A 32k x 8 device will conveniently store a field of one bit of data, so the PCB's accept two of these to store one frame.
Each single RAM card (Fig 5) can be tested separately and the memory expanded bit by bit (Pun intended !) as circumstances allow. A commercial system would no doubt have all the memory on a single high density board, but in this way it can be built by the average constructor, without too much worry about exceedingly fine tracks. For testing, RAM modules can be readily interchanged.

In order to use the memory two more modules are needed. These generate the read addresses (Fig 6) and the write addresses, plus arbitration logic (Fig 7) respectively. The arbitration logic is needed to interleave the read and write operations so that the system does not attempt to read and write at the same instant. By having separate read and write addresses the outgoing picture can be differently timed to the ingoing one, which is one of the main uses of a framestore. By stopping any further write signals, of course the memory will continue to read the existing data - i.e: a freeze frame.

The read address card has first to generate line blanking and a clock

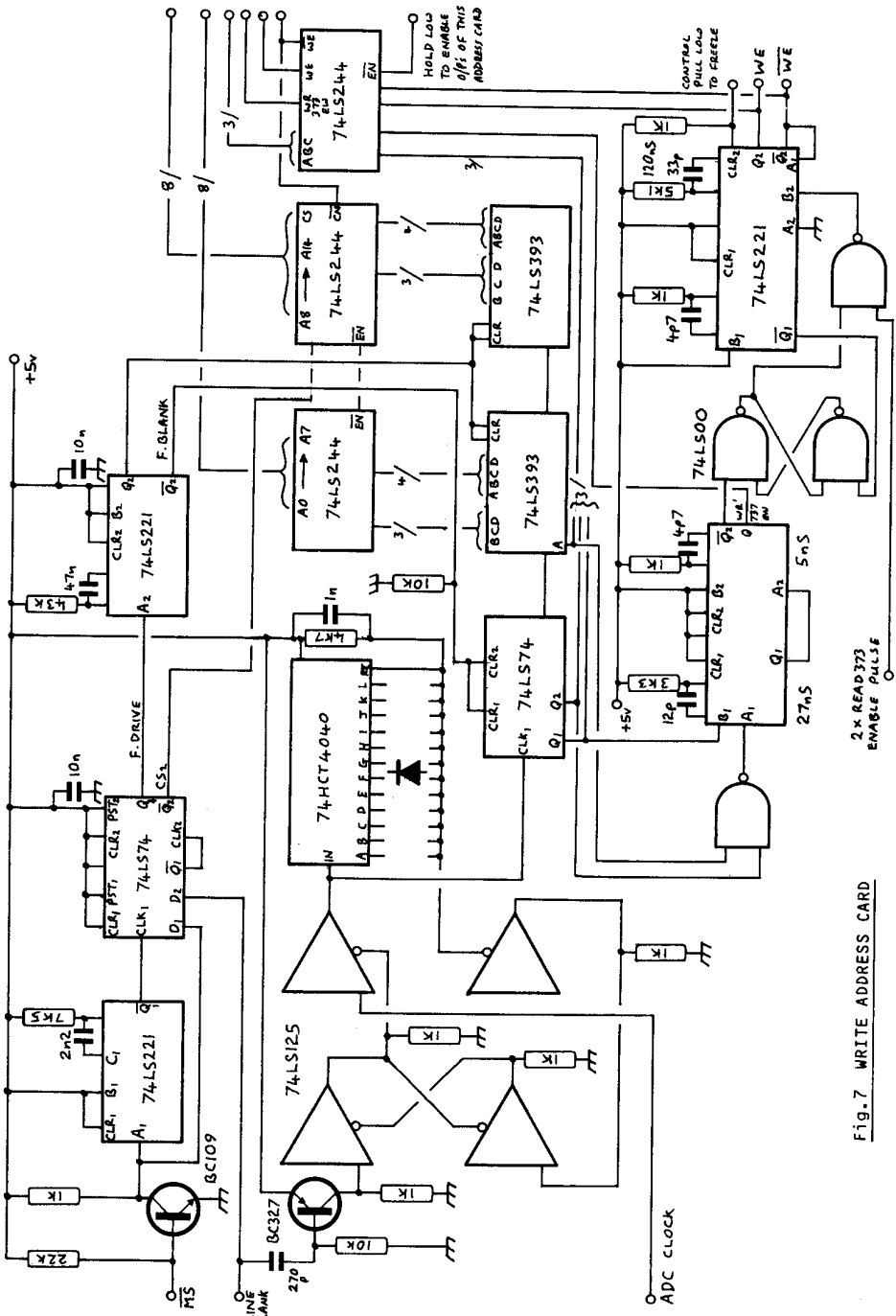


Fig.7 WRITE ADDRESS CARD

pulse locked to the sync pulses timed to suit the outgoing video signal. This is done in a very similar way to the incoming video clock pulses generated on the A-D / D-A card. The comparator inputs are reversed so its output is now non-inverted sync pulses. The positioning of the diodes and choice of NE564 oscillator capacitor are as described above.

Both address cards must count the appropriate number of clock pulses for the active part of each line (910 in the example worked through above). These must begin at the end of the line blanking period. The line blanking signal sets an R-S bistable, which allows clock pulses to a 74HCT4040 counter. This is programmed to divide by the number of pixels in the active line (910) and its output resets the R-S bistable, inhibiting the clock pulses until the next end of line blanking. The clock pulses also go to a counter chain made up of an 74LS74 and two 74LS393's, which generate the address codes for the memory boards. These counters are reset to zero by the frame blanking signal (inverted for the 74LS74). The address codes are buffered by the 74LS244's before joining a common address bus.

READ ADRRESS CARD		WRITE ADDRESS CARD	
PIN	CONNECTION	PIN	CONNECTION
1	+ve Supply	1	+ve supply
2	373 Enable pulse o/p	2	Freeze control
3	CS-2	3	CS-2
4	A14	4	A14
5	A10	5	A10
6	A13	6	A13
7	A9	7	A9
8	A12	8	A12
9	A8	9	A8
10	A11	10	A11
11	Ground	11	Ground
12	Ground	12	Ground
13	A7	13	A7
14	A6	14	A6
15	A2	15	A2
16	A5	16	A5
17	A1	17	A1
18	A4	18	A4
19	A0	19	A0
20	A3	20	A3
21	Enable 244 O/P's	21	Enable '244 O/P's
22	A 151 Clock I/P	22	A 259 Clock O/P
23	WE Input	23	WE Output
24	B 151 Clock I/P	24	B 259 Clock O/P
25	C 151 Clock I/P	25	C 259 Clock O/P
26	Line Blank Out	26	WE Output
27	MS	27	373 Enable Input
28	Read 373 Enable	28	Write 373 Enable
29	244 Enable (Card Select)	29	244 Enable(C/S't)
30	Spare	30	Line Blank I/P
31	DAC Clock Output	31	ADC Clock Input
32	Video/Sync Input	32	MS

TABLE.2 EDGE CONNECTOR DETAILS FOR READ AND WRITE ADDRESS CARDS

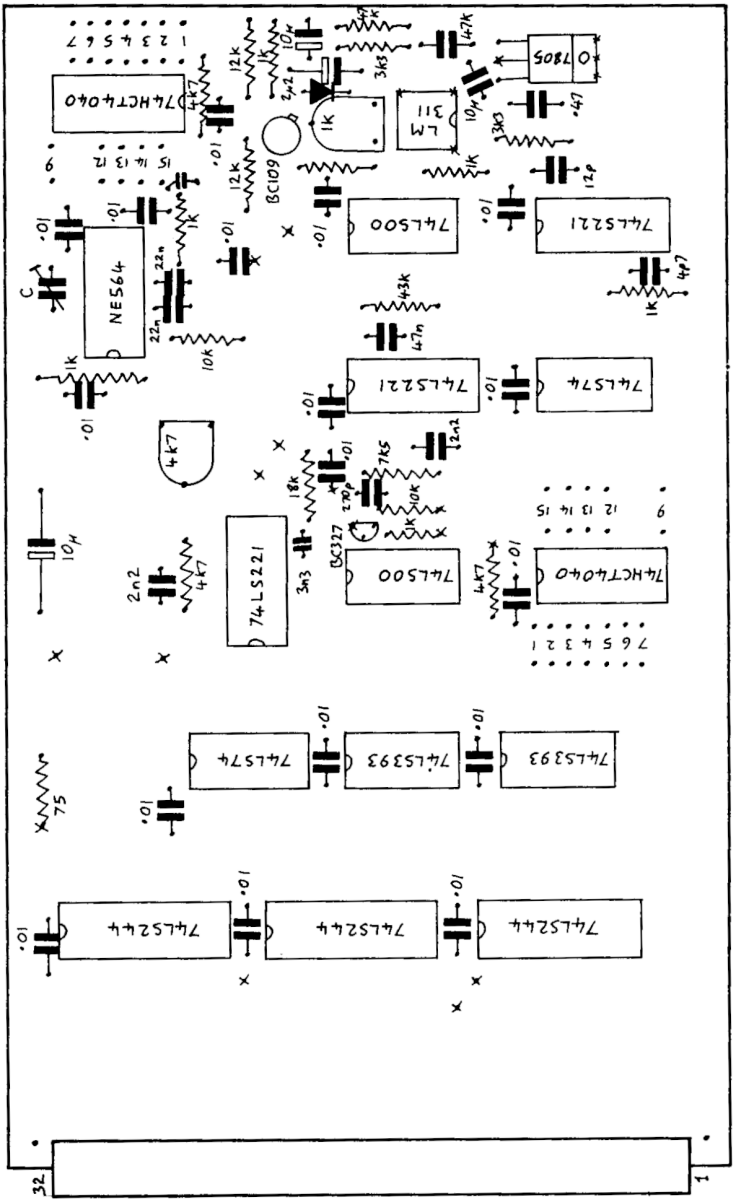


Fig.8 READ ADDRESS CARD

The address cards must also determine when the next set of eight samples is to be transferred in or out of the RAM. They must also ensure that only one of these tasks is tried at a time. This is done by setting the 74LS244's into the high impedance condition, except when their output is needed. All of this is done by the arbitration logic. Firstly, each set of addresses includes 3-bits that are used for the 74LS259's or 74LS151's for write and read respectively. On a count of eight, new data is transferred between these ic.s and the 74LS373 latches on the RAM card. The arbitration logic detects this count of eight (using the gate in the 74LS221 monostable) and then produces a short pulse to effect the transfer. The write address signals that the latch is full and waiting to update the memory. The arbitration logic waits until the 'read from memory to latch' pulse, whose falling edge triggers a monostable to generate a write enable pulse. This then resets the R-S bistable (via a short monostable) to await the next write pulse. The write enable pulse puts the write address onto the address bus and tells the RAM to load new data, before returning to the read state. If the monostable which generates the write enable pulse has its clear pin held low, then the monostable will not change state, even if a 'request to write' signal arrives at the input. When this happens the store remains in a read only state - i.e. it generates a 'freeze frame'.

NOTES: 1) Capacitors C connected to the NE564's on both Read and Write Address boards are adjusted as explained in the set-up explanation for the ADAC board given earlier. Similarly the 74HCT4040 programming diodes are selected as for the ADAC board.

This all makes a basic monochrome framestore which can be used, for example, to synchronise a non-genlocked picture source. There are two ways in which such a system may be expanded.

Firstly, if the samples are reassembled in a different order, or at a different speed, then the picture will be changed in either shape or size (a process called 'warping'). To do this, a suitable set of address codes would need to be generated and put on the address bus. In addition, as each new pixel does not correspond to a single pixel of the input signal, the output signal at each point needs to be composed of part of several adjacent pixels of the incoming signal. This is not a simple task - although a dedicated image resampling sequencer integrated circuit (such as the TMC2301 made by TRW) will help those wishing to experiment.

Secondly, the frame store may be expanded to handle colour pictures. As the timing of the input and output signals is not coincident (especially if the picture is warped) it is not practical to handle an encoded colour signal. For digital colour work the component signals need to be sampled and stored in memory and then coded once returned to analogue form. The eye does not see fine detail in the colour of the image so the R-Y and B-Y signals can be sampled at half the rate of the Y signal (and both stored, interleaved, in the same amount of RAM as the monochrome signal. The principle is shown in the block diagram (Fig 10). The coder, and (especially) decoder will need to produce exceptionally clean signals to avoid problems of aliasing (patterns produced by the interaction of the sampling frequency and the colour subcarrier).

Printed circuit boards may be available for this project, please consult your latest copy of CQ-TV for details. Alternatively, you may write to Members' Services enclosing a stamped address envelope.

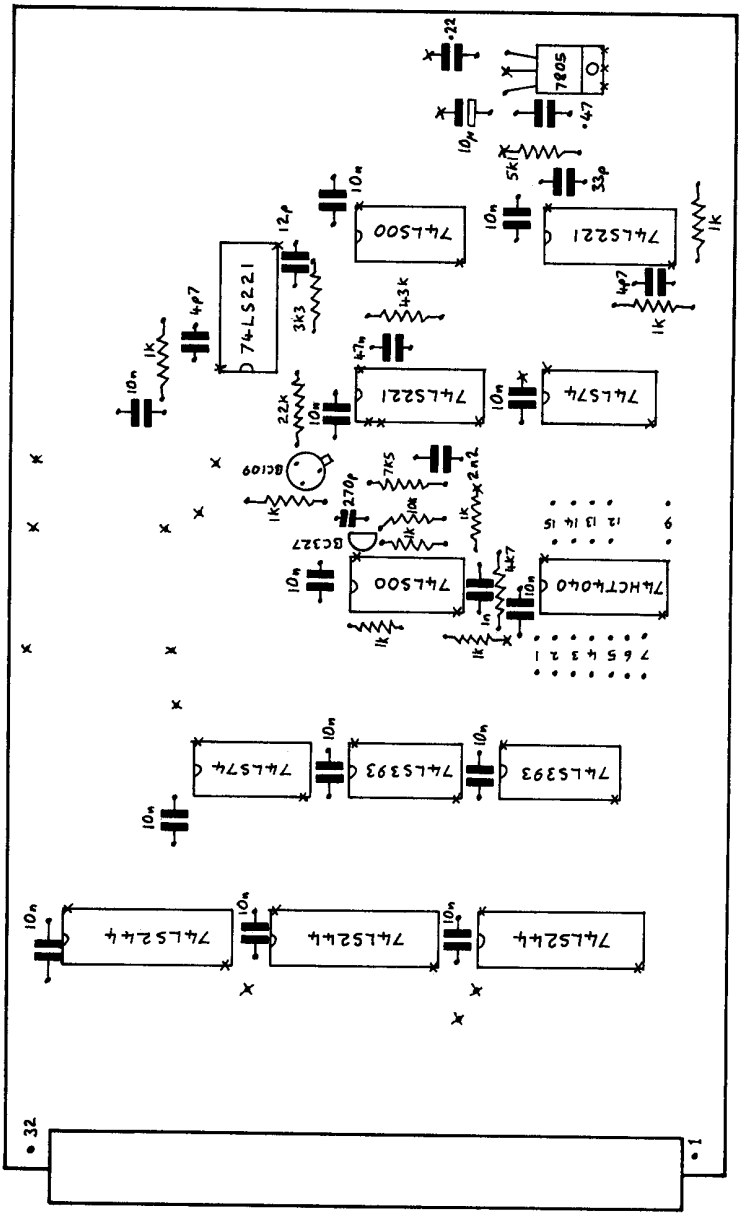


Fig.9 Write Address Card

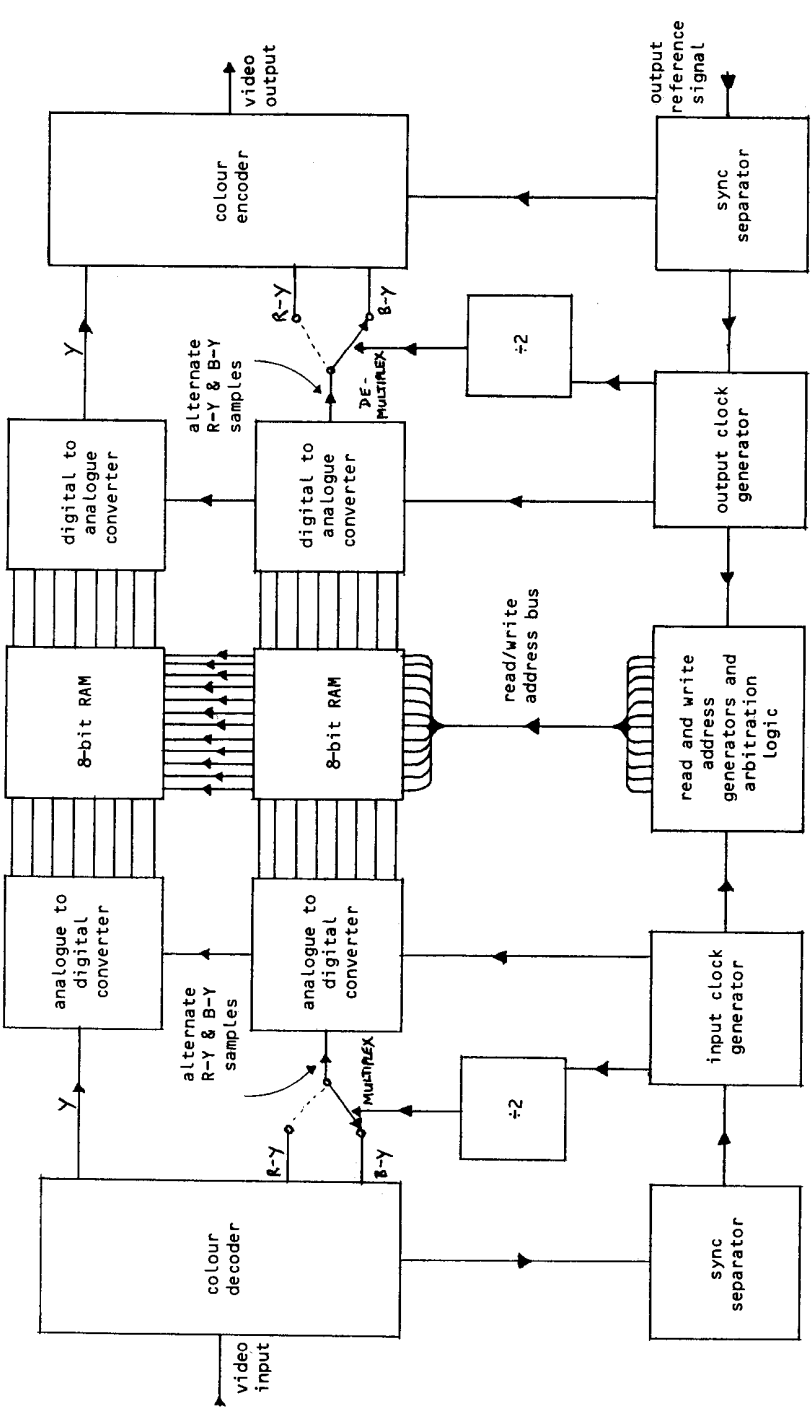


Fig.10 COLOUR FRAME STORE BLOCK DIAGRAM

A UNIVERSAL SYNC GENERATOR

This design is based on two special integrated circuits from Motorola. The SAA1043 is a universal sync pulse system which generates the synchronising waveforms required in all types of video source equipment (video cameras, film-scanners, video games, computer displays and general amateur TV equipment). The device is programmable to suit standards SECAM 1, SECAM 2, PAL/CCIR, NTSC 1, NTSC 2, and PAL-M; the video game 624 and 524-line standards; and can be synchronised to an external sync signal.

The SAA1044 is a subcarrier coupler which maintains the correct relationship between subcarrier and horizontal scan frequencies when an exact coupling is required. It is for use in combination with sync generator SAA1043.

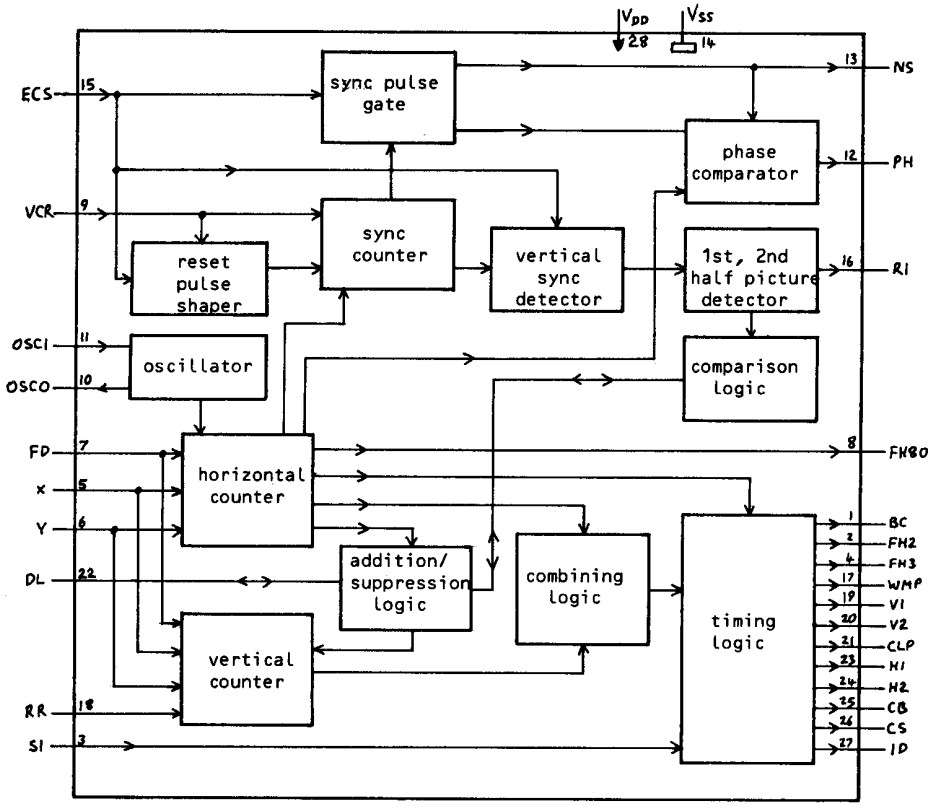


Fig.1 SAA1043 block diagram

The design described here is may be considered as a 'basic' unit programmed for 625-line PAL/CCIR operation. The circuit uses both devices and thus provides all the necessary output signals required for full colour applications. The design caters for either internal sync generation or genlocking to an external source. On 'internal' the subcarrier is held in the correct relationship to the horizontal scan frequency, however on 'external', because the incoming subcarrier is not also locked to the SAA1044 this relationship is not necessarily maintained. It is possible though to genlock the incoming subcarrier to this IC as we shall see later.

SAA1043 SYNC GENERATOR

The sync generator's features include an oscillator which functions with either LC or crystal elements; additional colour outputs to simplify camera signal processing; it can be synchronised to an external sync signal; vertical reset for fast vertical lock; subcarrier lock in combination with subcarrier coupler SAA1044; very low power consumption.

TABLE 1 - SAA1043 pinning

PINNING		
1	BC	burst flag/chroma blanking (SECAM) output
2	FH2	PAL identification output
3	SI	set identification input (SECAM, PAL, PAL-M)
4	FH3	400Hz (PAL); 360Hz (NTSC, PAL-M) and fH/3 (SECAM)
5	X	standard programming input
6	Y	standard programming input
7	FD	standard programming input
8	FH80	80 x fH output (1.25MHz)
9	VCR	VCR standard input
10	OSCO	oscillator output
11	OSC1	oscillator input
12	PH	phase detector output
13	NS	no-sync detector output
14	Vss	negative supply voltage (ground)
15	ECS	external composite sync input
16	RI	vertical identification output
17	WMP	white measurement pulse output
18	RR	vertical reset input
19	V1	vertical drive output
20	V2	vertical drive output
21	CLP	clamp pulse output
22	DL	2 x fH input/output
23	H1	horizontal drive output
24	H2	horizontal drive output
25	CB	composite blanking output
26	CS	composite sync output
27	ID	SECAM identification output
28	VDD	positive supply voltage

Fig.1 shows the internal block diagram which illustrates how the various parts of the IC function. This should help constructors decide what facilities, other than those included in this design, they require. Table 1 details the function of each pin.

PROGRAMMING OF OPERATING STANDARD

The standard required for operation is programmed using the inputs X, Y and FD as shown in table 2. The FD input selects 525 or 625-line working of the vertical counter and also influences the choice of oscillator frequency as shown in table 3

TABLE 2 - operating standard programming

standard	FD	X	Y
SECAM 1	0	0	0
SECAM 2	0	0	1
624	0	1	0
PAL/CCIR	0	1	1
NTSC 1	1	0	0
NTSC 2	1	0	1
524	1	1	0
PAL-M	1	1	1

positive logic: 1 = HIGH; 0 = LOW

OSCILLATOR

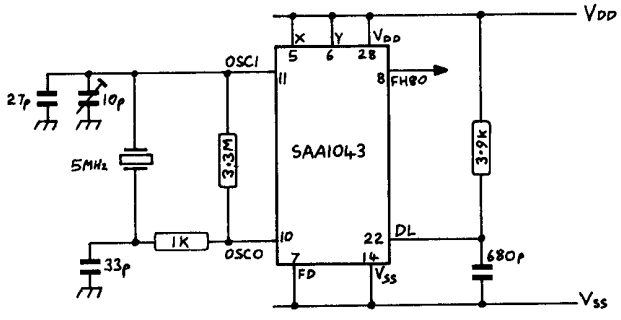


Fig.2 Crystal oscillator circuit

The built-in oscillator of the SAA1043 functions with an external LC-circuit as shown in the main circuit diagram (Fig.7) or with a crystal of the parallel resonance type (Fig 2). For operation in the VCR mode the LC oscillator circuit is recommended as it has a wider pull-in range when compared with the crystal. The frequencies required for the various operating standards are shown in table 3.

TABLE 3 - oscillator input frequencies

operating standard	osc.freq. MHz	vertical divider	vertical freq.Hz	horizontal freq. Hz
PAL, SECAM, 624	5.0	0	50	15625
NTSC, PAL-M, 524	5.034964	1	59.94	15734.26
PAL, SECAM, 624	2.5	H2 (pin 24)	50	15625
NTSC, PAL-M, 524	2.501748	H1 (pin 23)	59.94	15734.26

SYNCHRONISING TO AN EXTERNAL SYNC SIGNAL

Use is made of the phase comparator output PH to lock the internally generated sync pulses to an external sync signal. Reset pulses derived at each falling edge of the external sync signal (ECS) reset the sync counter which is clocked at the internal horizontal frequency by the horizontal counter. At each horizontal scan period the sync counter opens the sync pulse gate and allows the ECS to be applied to the phase comparator where it is compared with the phase of the internally generated horizontal sync pulse. When the two signals are in phase the output PH is in a high impedance state. When a phase

difference exists PH is pulled towards VDD or VSS depending on the direction of the error. The phase-analogue voltage on PH is used to correct the frequency at OSCI via a voltage-controlled oscillator and null the phase error between internal and external signals. Pulses occuring on the ECS outside of the sync pulse gating time (serration and equalisation pulses) do not effect the phase comparator.

Fig.3 shows the basic synchronising circuit using a passive filter network.

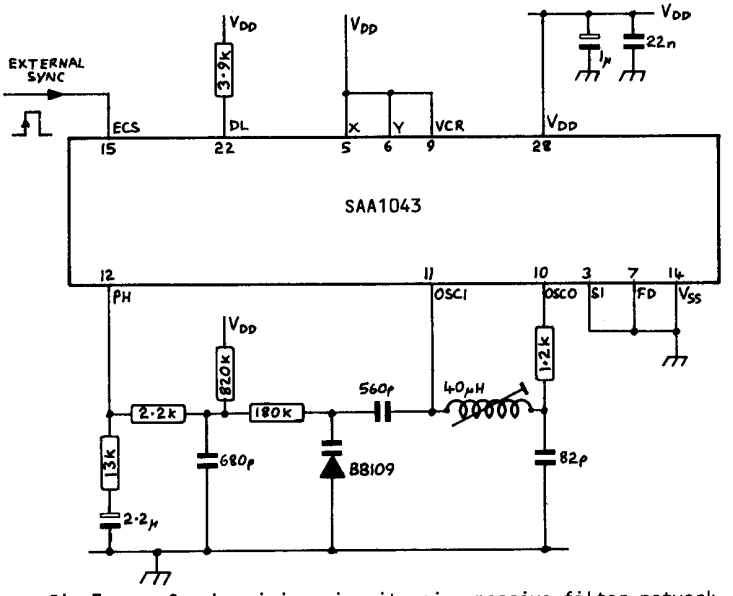


Fig.3 Synchronising circuit using passive filter network

SAA1044 SUBCARRIER COUPLER

The features of this device include the provision of an exact relationship between subcarrier and horizontal scan frequencies; accommodates all standard frequencies and facilitates genlock applications.

Fig.4 shows the internal block diagram which illustrates how the various parts of the IC function, and table 4 lists the function of each pin.

PROGRAMMING OF OPERATING STANDARD

The standard required for operation is programmed using the inputs FD, X and FH3 as shown in table 5.

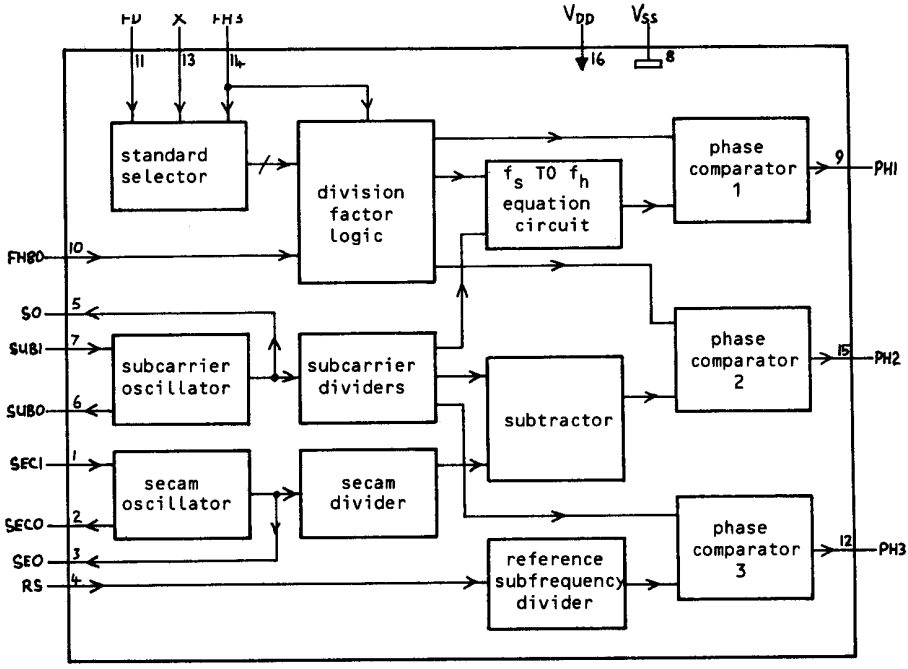


Fig.4 SAA1044 block diagram

SUBCARRIER/HORIZONTAL SCAN FREQUENCY RELATIONSHIP

The input FH80 from SAA1043 is the reference for horizontal scan frequency (fH). This frequency is reduced by a factor determined by the selected operating standard to give a value of 8fH (PAL, SECAM) or 10fH (PAL-N, PAL-M, NTSC) to phase comparator 1. The subcarrier frequency (fS) is manipulated to provide a comparable value at the second input to the phase comparator. When the frequencies of the two inputs to phase comparator 1 are equal, the relationship between fH and fS is as shown in table 5.

Phase comparator 1 functions with an exclusive-OR phase detector circuit and provides an output which may be used to control a voltage-controlled oscillator (VCO) via a low-pass filter. The VCO reference can be the subcarrier or the horizontal scan frequency and the filter can be active or passive, depending on application.

A second subcarrier oscillator circuit is provided for SECAM operation. The operating frequency of this is centred on 272fH to give, when fS=282fH, comparable values of 5fH at the two inputs to phase comparator 2. A second VCO loop can be used to control the SECAM oscillator frequency.

The high degrees of accuracy and stability required for genlock

applications are met by phase comparator 3. This compares the internal subcarrier and external reference frequencies. To adjust the phase over 2 pi, this comparator has a linear characteristic over 4 pi. The output signal PH3 has a period time of fS/4 and a duty cycle of between 12.5% and 62.5% giving a sensitivity of 240 mV/rad. Errors due to temperature variation are minimised by symmetrical circuit and chip design.

TABLE 4 - SAA1044 pinning

PINNING		
1	SEC1	SECAM oscillator input (272fH)
2	SECO	SECAM oscillator output (272fH)
3	SEO	inverted SECAM oscillator output
4	RS	reference subfrequency
5	SO	inverted subcarrier oscillator output
6	SUBO	subcarrier oscillator output
7	SUB1	subcarrier oscillator input
8	Vss	negative supply voltage (ground)
9	PH1	phase comparator 1 output (FH80/SUB1)
10	FH80	1.25 MHz input (from SAA1043)
11	FD	standard programming input
12	PH3	phase comparator 3 output (RS/SUB1)
13	X	standard programming input
14	FH3	standard programming input (from SAA1043)
15	PH2	phase comparator 2 output (SEC1/FH80)
16	VDD	positive supply voltage

TABLE 5 - operating standard programming

standard	FD	X	FH3	relationship of subcarrier frequency (fS) to horizontal scan frequency (fH)
PAL	0	1	400 Hz	fS = 283.7516fH
SECAM	0	0	don't care	fS = 282fH
PAL-N	1	1	400 Hz	fS = 229.2516fH
PAL-M	1	0	1	fS = 227.25fH
NTSC	1	0	0	fS = 227.5fH

positive logic: 1 = HIGH; 0 = LOW

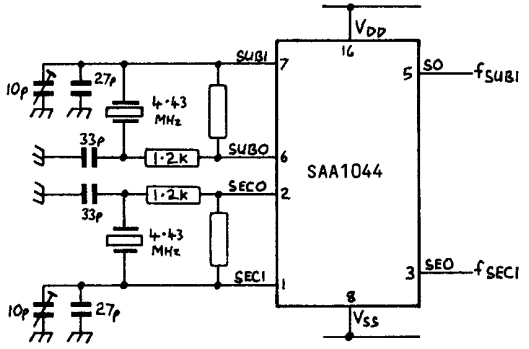


Fig.5 Test circuit for frequency measurement

Fig.5 shows a test set-up for oscillator frequency measurement whilst for those wishing to experiment in genlocking, Fig.6 shows an example of subcarrier coupling for PAL genlock application

PRACTICAL APPLICATION

Fig.7 shows the circuit of a sync generator with coupled subcarrier generator. Because the unit is to be used largely in amateur applications where sync pulses may not always be exactly correct, IC2 is provided with a LC oscillator. This means that sync signals from (say) a video recorder may be used and correct locking will still be maintained. A switch is provided to select either internally generated pulses or external locking.

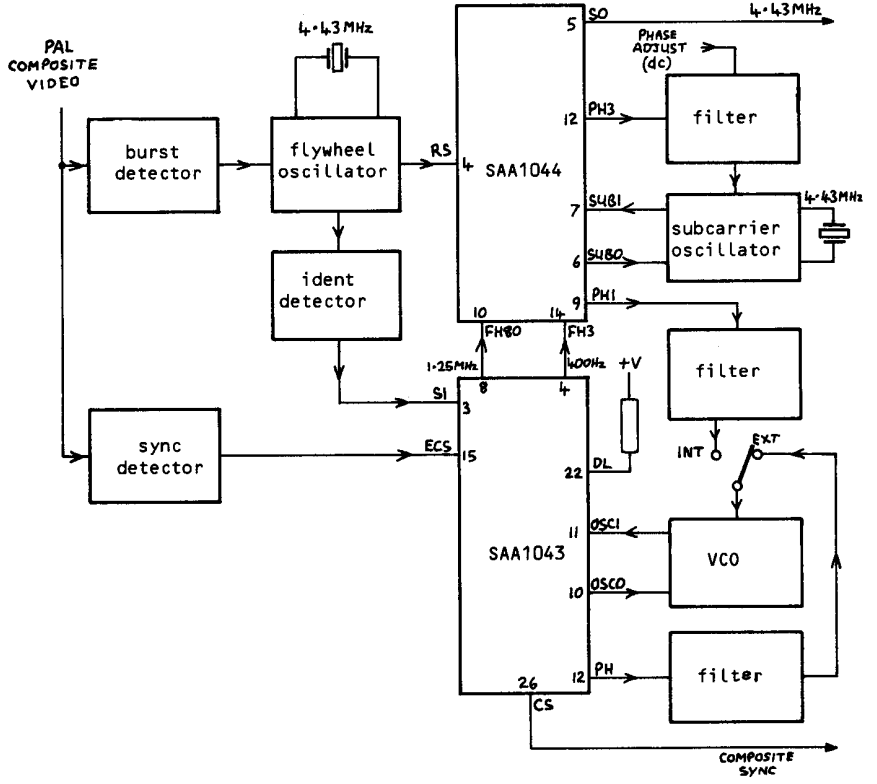


Fig.6 Subcarrier coupling for PAL genlock application

The outputs used in this design are all buffered and are made available at TTL level. If standard 2v p-p pulses across a 75-ohm load are required then a pulse amplifier should be provided on each output. A suitable pulse amplifier circuit is shown in Fig.8.

The subcarrier signal available from IC2 needs to be tailored before it is fed to a colour encoder. Fig.9 shows the circuit of a suitable processing amplifier. The subcarrier output from IC2 is buffered in Q1 and Q2 and a level control is provided in order that the required output level may be set. The signal passes through a filter to ensure that it emerges as a pure sine-wave which then goes to a linear output driver amplifier whose low output impedance may be terminated in 75-ohms.

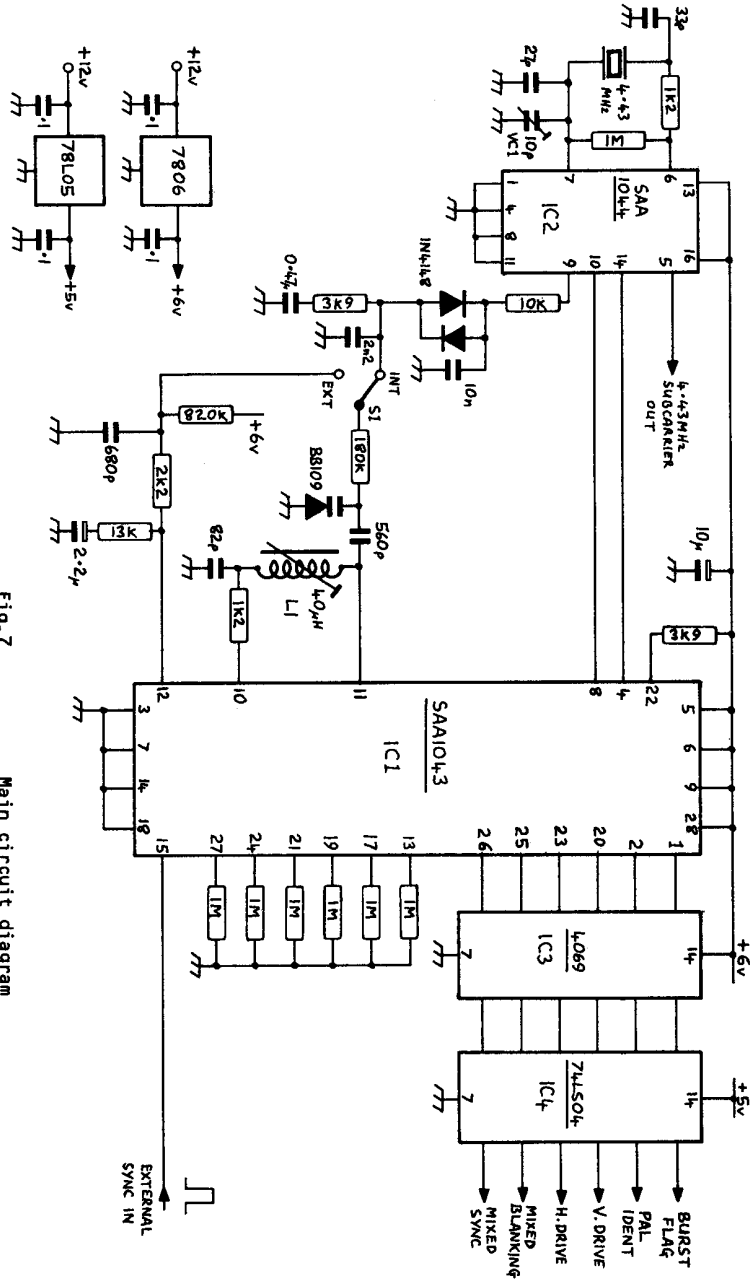


Fig.7 Main circuit diagram

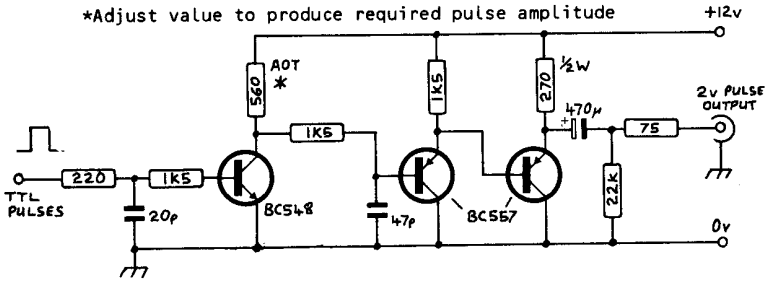


Fig. 8 PULSE OUTPUT AMPLIFIER

CONSTRUCTION

Owing to the experimental nature of this project and the multiplicity of options available to the constructor, a printed circuit board has not been made available at the time of writing (December 1988). However, if sufficient interest is shown a board could be produced in the future and this will be announced in CQ-TV in the 'Member's Services' lists.

The SPG/subcarrier coupler unit may be built on Vero stripboard or by manufacturing a printed circuit board. It is recommended that IC's 1 and 2 be fitted into sockets. The layout of both oscillators should be such as to ensure minimum lead lengths and mechanical stability of the components.

Several pulse output stages may be built on a single board or as separate amplifiers. The layout and wiring of these is fairly non-critical. Similarly the subcarrier processing board is not particularly critical although the filter components should be laid out in a symetrical manner.

COMPONENTS

IC1 is a 28-pin DIL and IC2 a 16 DIL. If a crystal is used for IC1's oscillator it should be of the parallel resonance type. The subcarrier crystal may be of the type commonly used in domestic TV sets. The manufacturer's application circuit shows the two diodes associated with pin 9 of IC2 as types BA318, however ordinary switching diodes type 1N4148 or 1N914 should be suitable. The two trimmer capacitors may be of the popular plastic Mullard type. For the 40uH variable inductor used in the LC oscillator option, a Toko 7P adjustable choke may be used, its stock number is 119ANA5870HM (orange).

Components for both the pulse amplifiers and subcarrier processor are fairly non-critical, however the filter inductors may be Toko fixed inductors (chokes) whilst the filter capacitors should be good quality types such as Polystyrene. Ceramic components are not normally recommended for filter circuits. The 330R emitter resistor in the subcarrier output circuit should be a 0.5W component whereas all others may be 0.25W rating or similar. The subcarrier level control may be a PC mounted preset type.

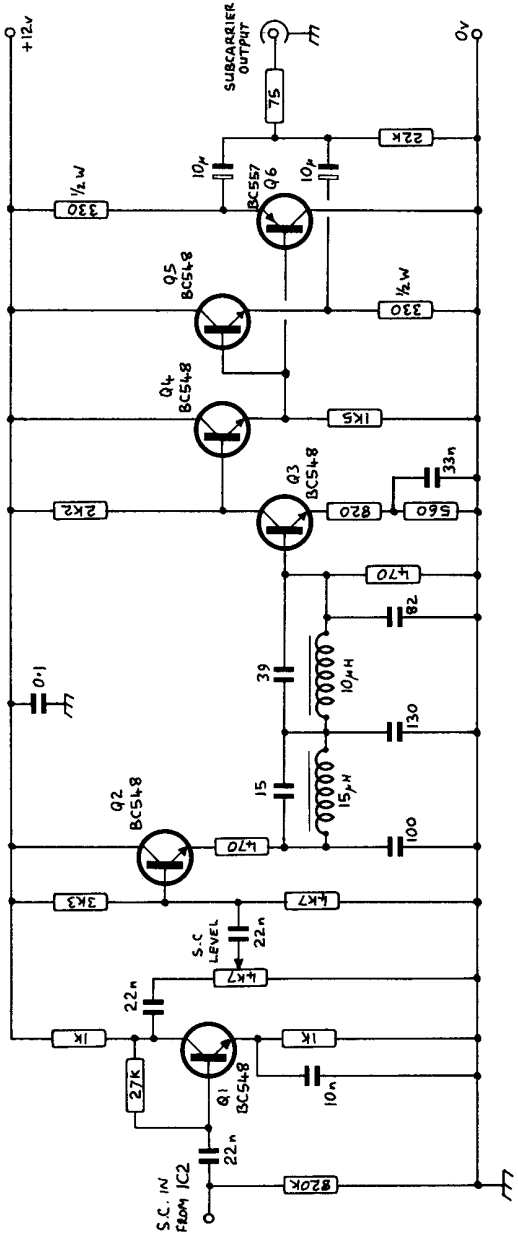


Fig.9 SUBCARRIER PROCESSOR CIRCUIT

SETTING-UP

There is very little setting-up to be done on the main unit (Fig.7), however the following points should be noted:

After switch-on check that the correct voltages are available on both the supply and ground (Øv) pins of all IC's. Switch S1 to 'int' and ensure that the various waveforms are available at the outputs of IC4. Connect a digital frequency meter to pin-8 of IC1 and, after a 15 minute warmup, adjust L1 so that it reads 1.25MHz. Connect the frequency meter to IC2 pin-5 and adjust VC1 to read 4.433619MHz.

The 5MHz oscillator is normally phase locked to the subcarrier generator and should pull in and settle within a few seconds. However, an indication of phase locking may be obtained by measuring the dc voltage on IC2 pin-9 and, ensuring that switch S1 is in the 'int' position, adjust L1, whereby the voltage should rise and fall accordingly. The best setting is for around half the available voltage.

Terminate the output of each pulse output amplifier (Fig.8) in 75-ohms and measure the pulse amplitude across the termination using an oscilloscope. The 'AOT' resistor should now be altered in value to produce the required output level for each amplifier.

Having connected the subcarrier output from IC-2 to the subcarrier processor shown in Fig.9, terminate the subcarrier output in 75-ohms and monitor the level with an oscilloscope. Adjust the 'SC level' control to provide 1v p-p on the 'scope. Check that the subcarrier waveform is a pure sinusoid. If it is not then check each stage to determine where the distortion is occuring.

SPECTRUM E-PROM PROGRAMMER

The E-prom programmer described here, for use with the Spectrum range of computers, will only program the larger E-Proms, which are now so inexpensive that they can be considered for most tasks. The design is very simple from a hardware point of view, most of the work being carried out in software.

HARDWARE

This design uses the very useful 8255PIO interface device. This chip has 24 Input/Output lines and allows much of the work normally carried out in hardware to be passed to software. The circuit is very simple, the prototype was built onto a piece of Vero board in a single evening. The power rails for the unit come from the Spectrum, apart from the programming voltage for the E-Prom, which is +21v for the standard 2732, and +12.6v for 27C128 and 27128A devices. If in doubt try the lower voltage first.

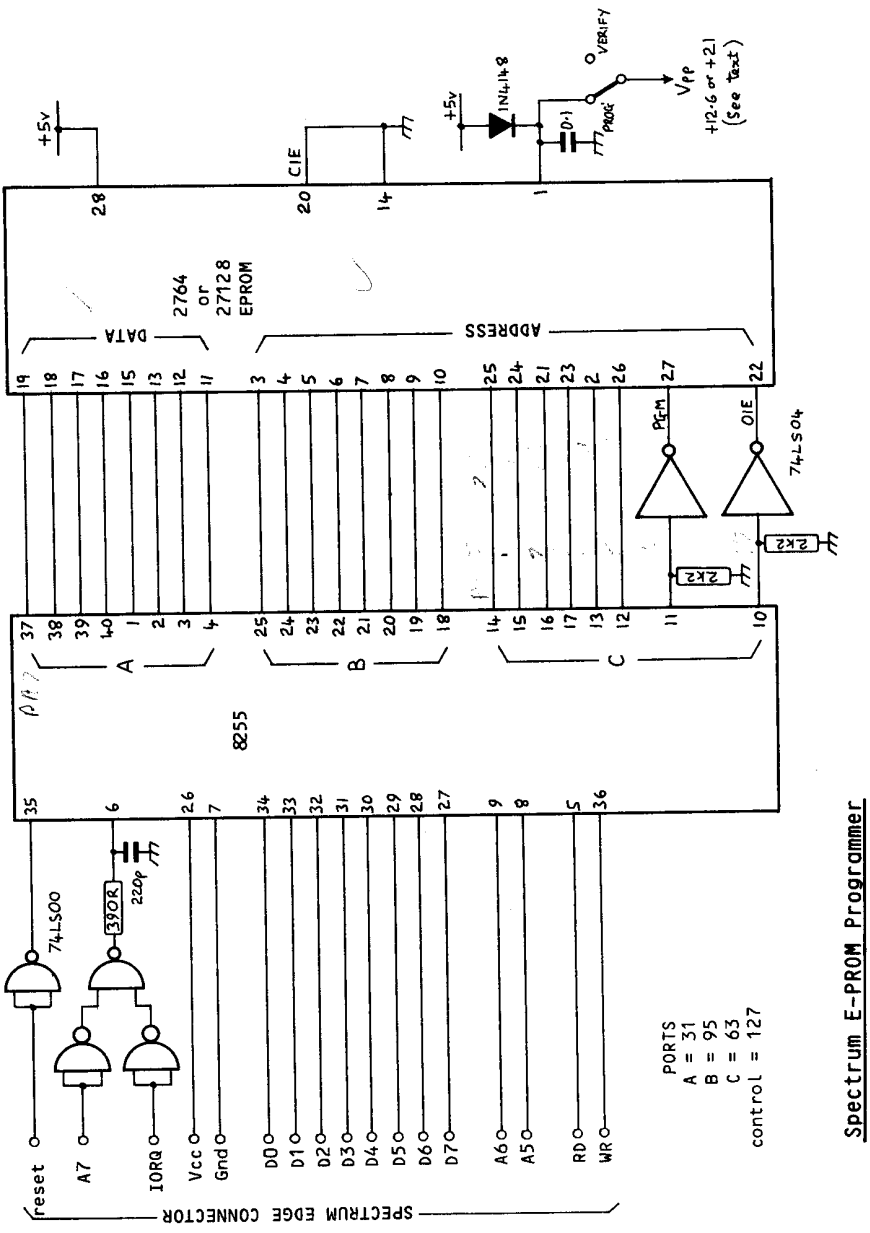
The output enable and programming control input (PGM) are connected via 74LS04 inverters, which have their inputs pulled low by 2.2k resistors. This is, perhaps, the only unusual feature of the hardware. When the PIO is first powered up the three ports default to inputs, the pull-down resistors ensure that the inverter inputs are low, and hence the output enable and PGM are high, which is the safest default position. The PIO is often re-initialised by the programming part of the software in order to reverse the direction of port-A from programming to reading. This change of direction will default the addresses carried by ports-B and C to zero, and were it not for the inverters the output enable and PGM would also be low, which would cause a data bus clash with a program pulse at address zero. The machine code program will soon move things out of this undesirable default state, but the inverters ensure that the E-prom data bus is tri-state, and that the programming pulse is high, so problems do not arise.

I have indicated on the circuit diagram (Fig.1) the port addresses for the 8255 should you wish to use it to interface other projects to your Spectrum. The addresses are in decimal so that Spectrum Basic can be used.

SOFTWARE

The machine code program which does all of the work is too long to reproduce here, a copy of it can be obtained from me at the address shown at the end of the article. The program resides just above basic and the E-Prom data is stored in memory from location 28000. When the software is loaded and run you are presented with the following menu:

LOAD A PROM INTO MEMORY	1
BLOW A 2764 PROM	2
BLOW A 27128 PROM	3
LOOK AT MEMORY	4
ENTER BASIC	5



Spectrum E-PROM Programmer

Option '1' will load either a 2764 or a 27128 E-Prom into the Spectrum's memory, so that data can be examined using option '4'. A 16k block of data is moved by the software, so if a 2764 (8k) is loaded into memory then the data will repeat after Hex 1FFF. This is not a problem and helps to keep the program simple and small (less than 1k byte).

When the program is first loaded the memory store is filled with logic 1's. This is useful for checking that an E-Prom has been erased and is in fact ready for programming (blowing). Insert the E-Prom and select option '2' or '3', dependant on the type, but do not switch on the programming voltage Vpp. This is the verify mode, where the E-Prom contents are compared with the contents of the memory store in the Spectrum. If all is well you will be returned to the menu, if not, a failure message will result giving the address at which the first problem occurs. This verify mode only takes a few seconds to check that an E-Prom has been correctly erased and is ready for programming.

To copy an E-Prom plug the master into the socket and select option '1', the contents of the master will now be duplicated in the Spectrum memory store. Replace the master with an erased E-Prom and select the appropriate option '2' or '3'. The E-prom will be verified as it is being programmed and should an error occur a failure message indicating the address of the error will be displayed. The programming voltage Vpp should be switched on before entering this mode and switched off when the menu returns. It may take as long as 15 minutes to program a device dependant upon the program size. I have not utilised any short-cut algorithms, each byte is read first and the 'blow' operation is skipped if not required.

Option '5' returns the computer to Basic so that the data in the memory store may be saved or recalled from tape or microdrive. The syntax required is:

```
    for a 2764 device      SAVE "FILE NAME" CODE 28000,8192
for a 27128 device        SAVE "FILE NAME" CODE 28000,16384
```

Microdrives require the extra syntax of:

```
    for a 2764      SAVE *"m";1;"FILE NAME"CODE28000,8192
   for a 27138      SAVE *"m";1;"FILE NAME"CODE 28000,16384
```

Saving files in order to store the data is a good habit to get into as it means that the Spectrum can be switched off during E-prom changes. This is not a problem if a microdrive is available for quick data storage and retrieval.

Files may be loaded into memory ready for programming by using the syntax:

```
                        LOAD "FILE NAME" CODE
or for microdrives          LOAD *"m";1;"FILE NAME"CODE
```

'RUN' will return you to the program from Basic, 'RUN 40' will clear the memory and load it with FF's.

The only option not on menu is verify. To check the contents of an E-Prom against memory use the program mode, but do not switch on the Vpp supply. If a failure message does not result then the contents of the E-prom agree with the contents of the memory which at switch on, or after 'RUN 40' will contain all logic 1's.

E-PROMS

For those of you not familiar with this means of data storage here are a few notes on E-Proms: An erased E-Prom contains a logic 1 in all its memory locations. To erase an E-Prom it must be exposed to ultra violet light of about 2537 Angstroms. This wavelength of light is readily available from the sort of UV lights used for insect control. Exposure to a small 8 Watt tube at a few inches for 20 minutes will erase the program and leave the E-Prom full of logic 1's (FF's). Erasure can be checked as stated earlier by using the look at memory mode after first loading the contents of the E-Prom into memory. To program the E-Prom the appropriate locations are then changed to loic 0 by the programmer, so that the programmed device contains a series of 1's and 0's which make up the binary words when read out by the processor or logic circuit in which they are to be used.

WARNING: Ultraviolet light at these wavelengths is dangerous to the eyes and skin, thus some form of opaque shielding should be used. Ozone can also be produced and inhalation may cause respiratory irritation.

DEVELOPMENT SYSTEM

This unit works well with the Hisoft Devpac assembler, where source code can be organised to run at any address and assembled under option 16. The object code saved to a microdrive or tape under command O. The computer can then be loaded with the E-Prom programmer software, the object code loaded to address 28000 and then programmed into the E-Prom.

For further information or a copy of the program please write enclosing an SAE to:

Trevor Brown, 14 Stairfoot Close, Adel, Leeds LS16 8JR.

GaAs FET CONVERTER FOR 24 CM AMATEUR TELEVISION

By G.Wehrhahn DD9DUK

This article first appeared in Elektor Electronics July/August 1988 and we thank the editors for permission to reproduce it here.

This 24cm down-converter is the perfect introduction to 24cm ATV, because it is a relatively inexpensive and simple design. It has only one preamplifier stage, an active mixer and a free running, single transistor, local oscillator. Construction is also fairly straightforward thanks to the use of a small printed circuit board with printed inductors (micro-striplines).

All prototypes of the GaAsFET converter were found to give better results than a formerly used combination of a two-stage stripline preamplifier for 24cm, using (very expensive) bipolar transistors type NE64535 from NEC, and a 24cm down-converter based on a crystal-controlled local oscillator chain and a Schottky diode mixer (designed by DJ5XA and described in edition 2/1975 of VHF Communications). Interestingly, the cost of the GaAsFET converter is much lower than this (now technically outdated) combination of a preamplifier and a converter.

CIRCUIT DESCRIPTION

The coming of Gallium-Arsenide semiconducters has enabled receiver noise figures to fall below values that are virtually impossible to achiCONV
ith bipolar transitors available to the radio amateur. The GaAsFET's used in the present converter are relatively inexpensive dual-gate types 3SK97. Types S3030 (Texas Instrumemts) and CF300 (Siemens) were also tried with excellent results.

Contrary to popular belief, there is nothing mysterious about GaAsFETs. In fact their outlook, static and dynamic operation is very similar to that of well-known VHF or UHF dual-gate MosFETs in the 3Nxxx and BF9xx series. The main advantage of the GaAsFET used here is that it can offer an in-circuit noise figure that remains below 2dB for frequencies up to 1.5GHz. Furthermore, gain is high but stable, and matching to tuned circuits is fairly simple thanks to the extremely low internal capacitance that results in a small reactive component.

The circuit diagram of the converter is shown in Fig.1. The incoming signal from the aerial reaches gate-1 of preamplifier T1 via micro-stripline inductor L2. Matching of the input stage to the cable impedance of 50-ohms is optimised by adjusting trimmer C2. Preset P1 allows the drain current of the FET to be adjusted to optimise the gain/noise figure of the device. In most cases a compromise between these two will have to be found. The amplified 24cm signal is passed to mixer T2 via a three-element top-coupled micro-stripline filter, which is tuned by means of trimmers. It should be noted that C10 and C12 increase the total bandwidth of the filter to a value suitable for reception of 27MHz wide FM ATV signals. For AM ATV these capacitors may be omitted to achieve pure inductive coupling resulting in lower bandwidth.

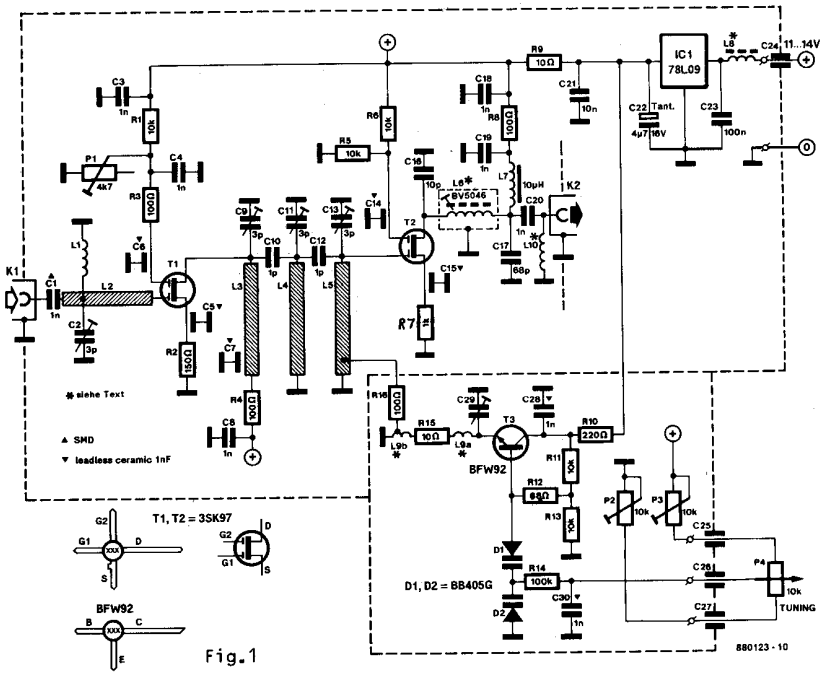


Fig.1

The local oscillator signal reaches gate-1 of T2 via R16 and a low impedance tap on L5. The intermediate output frequency of the converter can be chosen freely between 40 and about 200MHz. In prototypes the drain circuit of T2 was tuned to 48MHz by C16, L6 and C17 to enable the converter to be used for AM ATV reception with a portable colour set tuned to VHF channel-2 (now no longer used for broadcast TV in the UK). Provided C16, L6, C17 and L10 are dimensioned accordingly, the intermediate frequency is simple to move up to, say 180MHz (channel-6 in band 3). Obviously, the higher the intermediate frequency, the better the image rejection of the mixer. A domestic television set is, of course, not suitable for receiving FM ATV unless the resultant loss of quality in the FM to AM conversion is acceptable. For FM ATV a special intermediate frequency amplifier will have to be made, followed by a wide-band FM demodulator. The most commonly used IF for FM ATV is 70MHz, but here again, the IF frequency can be chosen freely.

Editor's note: If it is intended to use the BATC design FM demodulator (CQ-TV122 pp6-11) an IF frequency between 35MHz and 50MHz is desirable. If using a Wood & Douglas demodulator an IF around 50MHz is required.

The single transistor, varicap-tuned local oscillator is a slightly modified version of that discussed in Ref.1. Properly constructed,

its stability is so good that an AFC circuit is not required. Presets P2 and P3 enable defining the tuning range of the converter. Capacitor C29 is a course frequency adjustment, and also serves to stabilise the power output of the oscillator. This trimmer, which may not be needed in all cases, is simply 10mm or so of straight wire positioned above the PCB surface. Although not apparent from the circuit diagram, the actual length of the anode lead of D1 and the construction of L9a also determine the frequency of operation. The oscillator can be set to operate roughly between 1000MHz and 1500MHz. Finally, the dashed lines in the circuit diagram denote a screen around the local oscillator to prevent stray radiation.

CONSTRUCTION

Figure 2 shows the printed circuit board designed for the converter. By arrangement with Elektor Elektronics the BATC produces PTFE boards for this project and these are available from BATC Member's Services (details in CQ-TV magazine). In the description below, the upper drawing is called the component side, and the lower drawing the reverse side (soldering side would be incorrect because a number of components are soldered at the component side).

Construction is fairly simple for those accustomed to the use of the leadless ceramic capacitors. The actual value of these is uncritical (anything between 470pF and 1.5nF will work; 1nF being the most commonly available value). There are seven of these capacitors in the converter - each is fitted vertically in a slot which is carefully jig-sawed or drilled and filed in the PCB. The length of the slots is such that the shoulders of the leadless capacitors rest on the PCB surface. Be sure to cut the slots in the correct places. At first glance the rectangles indicated on the ground plane side appear to indicate their exact positions, whereas the slots are in fact cut to one side of these; the rectangles providing insulation between ground and the 'active' side of the trapezoidal capacitors. The holes for the two GaAsFETs are drilled to 3.5mm. T3 is not fitted in a hole.

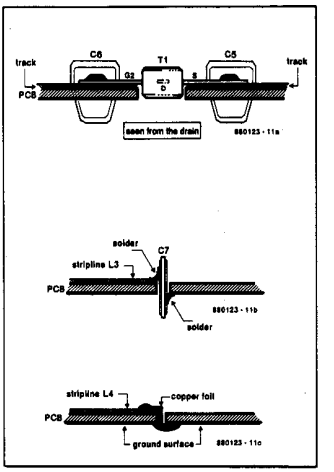
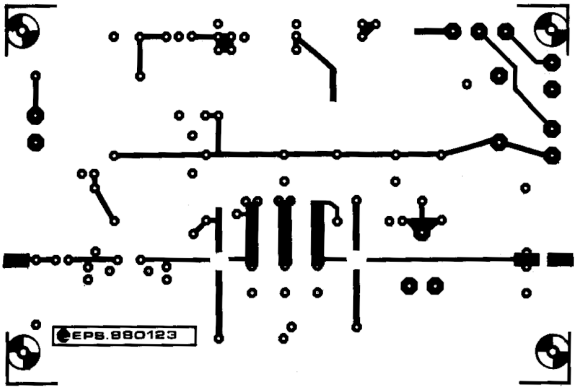


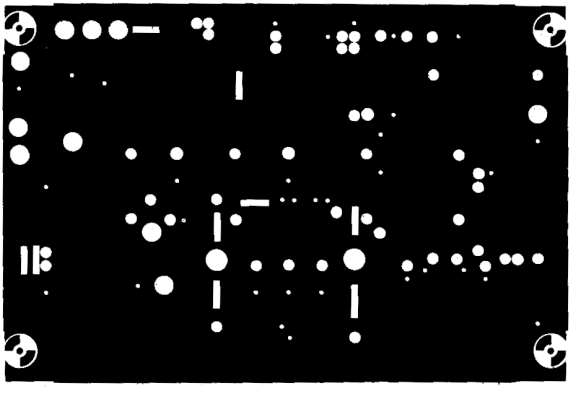
Fig. 3. Showing the use of leadless ceramic capacitors on the PCB (3a; 3b), and the connection to ground of micro-stripline L4 with the aid of a small piece of copper foil (3c).

The cross-sectional views of the PCB in Fig.3 show the connections of the gate-2 and source terminals of T1 to decoupling capacitors C6 and C5 respectively. Micro-stripline L4 is connected to ground by a small piece of copper foil. All 1nF capacitors (and C21) not marked with a black triangle in the circuit diagram are miniature ceramic types with a lead spacing of 2.5mm. Input inductor L1 is one turn of Ø.5mm diameter silver-plated wire. Choke L8 is wound as 6 turns of Ø.2mm dia. enamelled copper wire through a ferrite bead or small balun. Inductors L9a and L9b are formed by the wire terminals of R15. L9a is 2 turns with an inside diameter of about 3mm and a turns spacing of 1mm.

2 **Note: only T1, T2 and C1 are mounted at this side of the board**



(less than actual size)



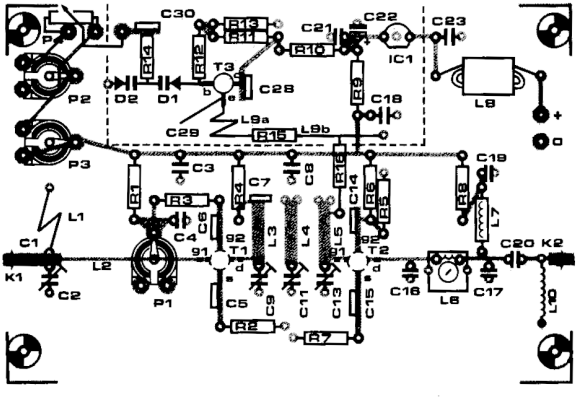


Fig. 2. Double-sided printed circuit board for the converter.

Parts list

Resistors (0.25 W carbon film; ±5%):
R1;R5;R6;R11;R13 = 10K
R2 = 150R
R3;R4;R8;R16 = 100R
R7 = 1K0
R9;R15 = 10R
R10 = 220R
R12 = 68R
R14 = 100K
P1 = 4K7 or 5K0 preset H
P2;P3 = 10K preset H
P4 = 10K linear potentiometer

Capacitors:
C1 = 1n0 chip or SMD (Bonex; VeroSpeed; Cirkit)
C2;C9;C11;C13 = 3p subminiature trimmer (manufacturer: Sky) (C-I Electronics)
C3;C4;C8;C18;C19;C20 = 1n0 ceramic
C5;C6;C7;C14;C15;C28;C30 = 1n0 leadless ceramic (Cirkit; Bonex)
C10;C12 = 1p0 (see text)
C16 = 10p
C17 = 68p
C21 = 10n ceramic
C22 = 4μ7; 16 V; tantalum
C23 = 100n
C24 . . . C27 incl. = 1n0 feedthrough (solder type) (Cirkit; Bonex)
C29 = see text.

Inductors:
L1 = see text.
L2;L3;L4;L5 = micro-stripline on printed circuit board.
L6 = Neosid BV5046 (yellow-blue; 0.9 μH; 5 . . . 50 MHz) (C-I Electronics).
L7 = 10μH axial choke.
L8 = see text.
L9 = see text.
L10 = see text.

Semiconductors:
D1;D2 = BB405G (Bonex; C-I Electronics)
IC1 = 78L09
T1;T2 = 3SK97 (C-I Electronics)
T3 = BFW92 (Cirkit)

Miscellaneous:
K1;K2 = BNC socket (flange type).
PCB Type 880123 (not available ready-made through the Readers Services).
Tin-plate box with top and bottom lids. Size: 111 × 74 × 50 mm.

The other inductor, L9b, is the straight-wire terminal soldered to ground, as shown on the component overlay. A 2mm hole is made in the screen surrounding the local oscillator, so that R16 can be soldered to a tap on L9b, approximately 10mm from where this is bent down and connected to ground. It is important that R15 runs horizontally at about 4mm above the PCB surface. Also make sure that it does not cause excessive strain on the emitter lead of T3.

When required, coupling capacitors C10 and C12 are fitted direct onto the micro-striplines, keeping the leads shorter than 1mm. The GaAsFETs are the last parts to be mounted on the PCB. As they are very small and static-sensitive, soldering must be done fast, with utmost care and using a low-power iron with a grounded tip.

The completed PCB is mounted in a tin-plate box (type 6, stock number 7760 - Piper Communications) with feed-through capacitors for the direct voltages and holes for the BNC sockets K1 and K2. These are positioned such that the centre pin can be soldered direct on to the copper area provided. The PCB edges at the reverse side of the board are soldered direct to the inside of the box panels. When a ready-made tin-plate box is not available an alternate enclosure can be made from cut-to-size pieces of printed circuit board. The screen around the oscillator is made high enough so that, when the board is mounted in its box, the top edge of the screen rests against the underside of the box lid.

NOTE: In the original component layout as reproduced in Elektor Electronics IC1 was shown reversed, this has been corrected in the layout shown here.

SETTING UP

The simplest way of aligning the converter is to ask for the assistance of a radio amateur to transmit ATV on 24cm. Alternatively, you may be in the service area of one of the several 24cm FM ATV repeaters operational in the UK, and thus tune up the converter using that signal. For the following description it is assumed that a 24cm ATV signal is available, and that the converter is used in conjuction with a TV set tuned to VHF channel-2, or a pre-aligned FM ATV demodulator with the video output fed to a monitor. (It must be noted that if a television set is used to receive the picture direct from the converter it will be degraded due to having to slope-detect the FM signal for the AM television).

Set all presets and trimmers to the centre of their travel. Adjust P1 for a drop of 1.3 volts across R2. Check that the oscillator works by measuring the drop across R7; short-circuit the emitter of T3 to ground to stop oscillation. This should cause the voltage drop across R7 to drop by about 0.2 volts. Remove the short circuit and peak L6 for maximum noise output of the converter, then tune to the ATV signal and peak the trimmers for optimum reception. This is fairly easy when the signal strength is relatively strong initially. Reduce the signal strength by carefully turning the receive aerial away from the transmitting station and redo all adjustments for the best reception. It may be necessary to bend C29 closer to the PCB, or space the turns of L9a wider, to stabilise the local oscillator output across the tuning range. Note, however, that re-positioning C29 changes the oscillator frequency, so that the tuning control P4 must be adjusted

to restore reception. Also, P2 and P3 may have to be readjusted to obtain the correct tuning range.

REFERENCE: 1) 'Indoor Unit for satellite TV reception, part-1.' - Elektor Electronics October 1986.

SPECIAL COMPONENTS

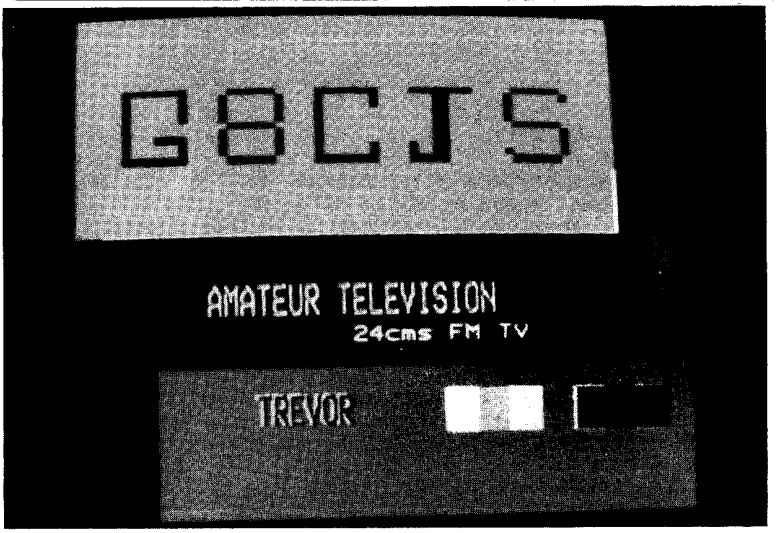
The special components required in this unit may be obtained from the following suppliers:

Chip capacitor C1 (1nF) - Bonex, Piper Communications
Trimmer capacitors C2, C9, C11, & C13 (3p) Sky type - Piper Communications
Trapezoidal (coffin) capacitors (1nF) C5, C6, C7, C14, C15, C28 & C30 - Bonex, Piper Communications
Feedthrough Capacitors (1nF) C24 to C27 - Bonex
Inductor L6 (0.9Uh) - Piper Communications, Wood & Douglas
Two-hole balun L8 - Bonex
Diodes D1 and D2 (BB405G) - Bonex
Transistor T3 (BFW42) - Bonex
78L09 regulator* - Piper Communications
GaAsFETs T1 and T2 CF300 Piper Communications
Tinplate box, type 6, stock number 7760 - Piper Communications

* NOTE: Due to the possible difficulty in obtaining 78L09 regulators, an alternative method would be to use a readily available 78L05 (R.S.Components stock no: 306 190) with a 3.9 volt zener diode between the reference leg and earth.

Bonex Ltd., 12 Elder Way, Langley Business Park, Slough, Bucks SL3 6EP. Tel: (0753) 49502

Piper Communications, 4 Severn Road, Chilton, Didcot, Oxon OX11 0PW. Tel: (0235) 834328



A 24CM FM TRANSMITTER

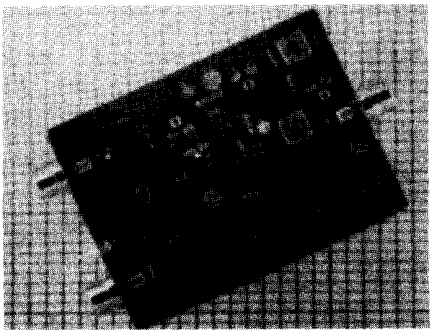
INTRODUCTION

The transmitter consists of two modules: a baseband video and audio modulator and a phase-lock-loop (PLL) exciter. The circuit is by Klaus Hirschelmann DJ7OO and was originally published in an article in 'Der TV-Amateur'. The original design has been augmented and modified to some extent so that the circuitry can be built as compactly as possible. The transmitter is extremely stable and produces an RF power output at around 1Ø mW.

BASEBAND AND AUDIO SUBCARRIER GENERATOR

The printed circuit is shown in Fig.1, a component layout in Fig.2 and the printed circuit board layout is shown actual size in Fig.3. A photograph of a completed board is reproduced below.

A 1 volt peak-to-peak (p-p) composite colour video signal is fed, via a 1ØØ-ohm deviation control, to a two-stage video amplifier. The output is routed through a standard CCIR pre-emphasis network.



The audio signal (1 volt maximum) goes to an operational amplifier stage with automatic gain control provided by a FET transistor. The gain of the op-amp is pre-set by the 1M potentiometer connected to pin-6. The output is fed to the varicap diode combination (BB2046) via a 1k audio deviation control.

A BF245C forms the subcarrier oscillator, the frequency of which is adjusted by the 5uH coil. The BF199 acts as an output buffer, feeding the modulated subcarrier through a filter and 1ØØ-ohm level control, to the baseband output where it mixes with the video signal.

The 72 x 53mm PCB (1.6mm epoxy, plated one side only) should be assembled and then fixed inside a standard 72 x 52 x 28mm tinplate box, as shown in Fig 4. Low cost phono sockets are used as input and output connectors. These are smaller than BNC's and are perfectly adequate for baseband signals. The 'tails' of the video and audio input, and baseband output sockets should be shortened a bit to avoid fouling other components and possibly causing short circuits. The 1N4ØØ3 polarity protection diode should be soldered vertically, direct to the +12V input, which should enter the tin box via a 1nF feed-through capacitor. The subcarrier filter coil BV5Ø56 can be replaced by a BV58ØØ if desired; the PCB layout has taken both types into consideration. The value of the parallel capacitor should then be reduced to about 82 pF.

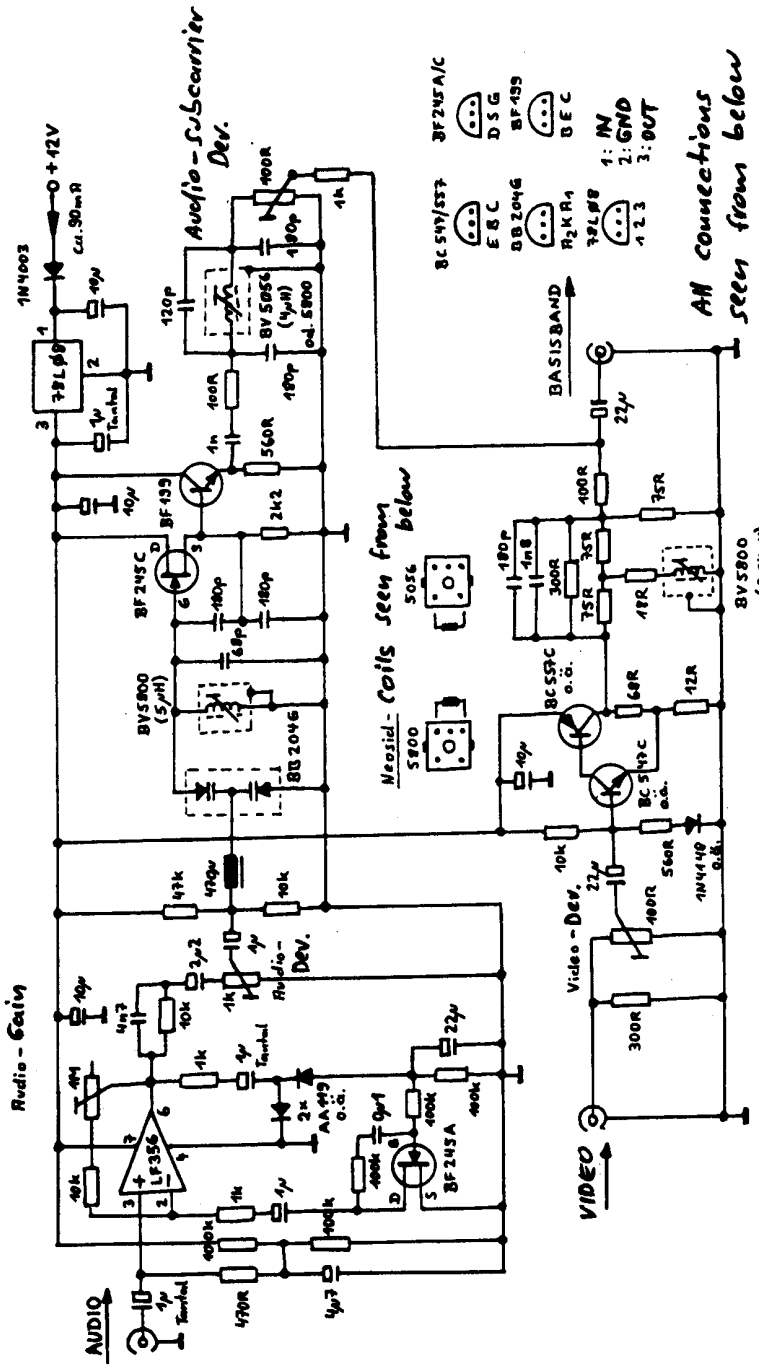


Fig.1 Baseband and Audio Subcarrier Generator.

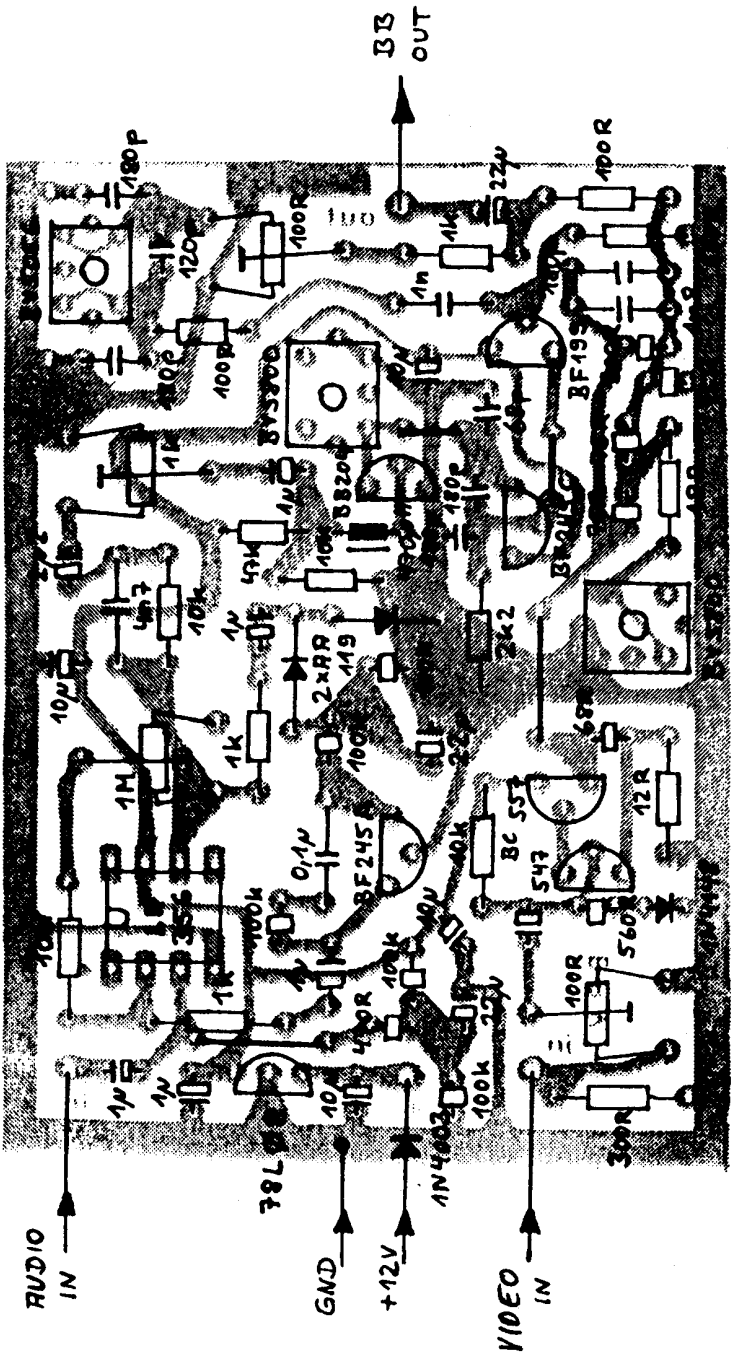


Fig.2 Baseband board component overlay.

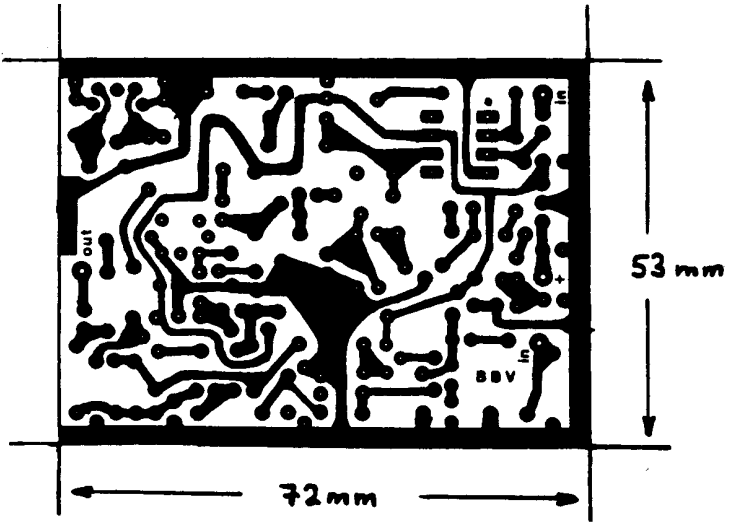


Fig.3 PCB layout of Baseband circuit (actual size).

PLL-LOCKED TRANSMITTER

The transmitter circuit is shown in Fig.5, with the PCB layouts in Fig.6 (shown actual size) and the component overlay in Fig.7.

The basis of the transmitter is a voltage controlled oscillator (VCO) configured around a BFR96 transistor. The VCO frequency is determined by a stripline inductor (L1) and a 5pF trimmer, and is controlled by the output of the phase-lock-loop IC SP5060. The PLL chip is in turn locked to an external crystal. This system provides very good frequency stability.

The baseband signal is routed to the VCO varicap diodes via a BC547 emitter follower stage. The modulated output from the VCO stage is fed to a monolithic microwave integratted circuit (MMIC). This high gain device amplifies the carrier and feeds it to the transmitter output through a three-stage stripline filter. A feed from the MMIC output is also taken to the PLL chip via a short coaxial cable.

The VCO and PLL sections of the circuit are screened by a dividing wall soldered across the tin-plate box housing the boards. They are connected together via feedthrough capacitors and a short coaxial lead. Both 72 x 36mm PCB's are made from 1.6mm thick epoxy material. The PLL board is single-sided whilst the VCO board is double-sided. The tin plate box for this assembly should be of appropriate size.

All components on the VCO board are surface mounted on the upper (tracked) side. The only drilling necessary is for components which need to be soldered to the groundplane (underside), and these are marked on the layout (Fig.7) with holes at the solder points. The surface mounted (SMD) capacitors indicated on the circuit diagram could be substituted by very small ceramic types. The three 1nF SMD capacitors connected around the PLL SP5060 should be soldered on the ground plane side of the board underneath the IC (see overlay Fig.8). The BFR96 VCO transistor and the MMIC are mounted in 3/16 inch holes

drilled through the printed board. The trimmers are Sky or Thorn 809 series.

The final output frequency is dependant on the frequency of the crystal in the PLL circuit. The frequency of the crystal is determined by dividing the transmit frequency by 256 (the multiplication factor of the PLL IC). For example: for a transmit frequency of 1249MHz (RMT2 repeater I/P) the crystal required will be

1249/256 = 4.879MHz

The locations of the holes for the input and output sockets etc. are shown in Fig.8. Three 1nF feedthrough capacitors should be fitted in the screen for the connections between the VCO and PLL sections. A small notch must also be cut into the screen as shown, after which it should be soldered into the middle of the case. A BNC flanged socket is used for the RF output, preferably soldered to the tin box. The teflon collar and pin should be shortened by about 3mm. The baseband input socket (BNC or phono) and the power input feedthrough capacitor should also be fitted at this stage.

Next, the already completed PCB's should be offered up to the underside of the box. The centre pin of the BNC RF output connector should now line up flush to the output track of the PCB. The wire 'tails' from the feedthrough cap's are joined to corresponding holes in the PCB. The boards can now be soldered to the side walls of the box and to the screen. For best heat dissipation, the voltage regulator should be smeared with thermal paste and bolted to the side of the box. A short length of miniature coax is used to connect the PLL board to the VCO on the underside, as shown in Fig.7.

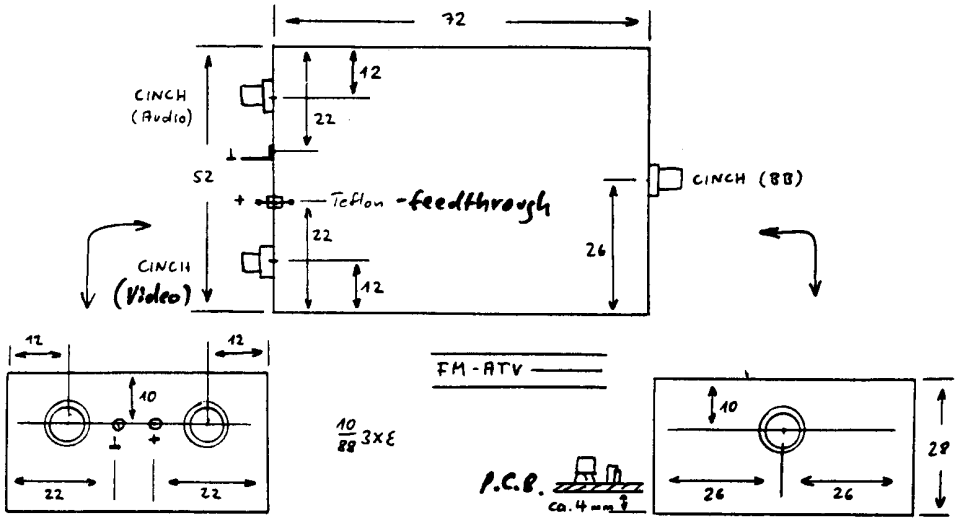


Fig.4 Enclosure details for Baseband Unit.

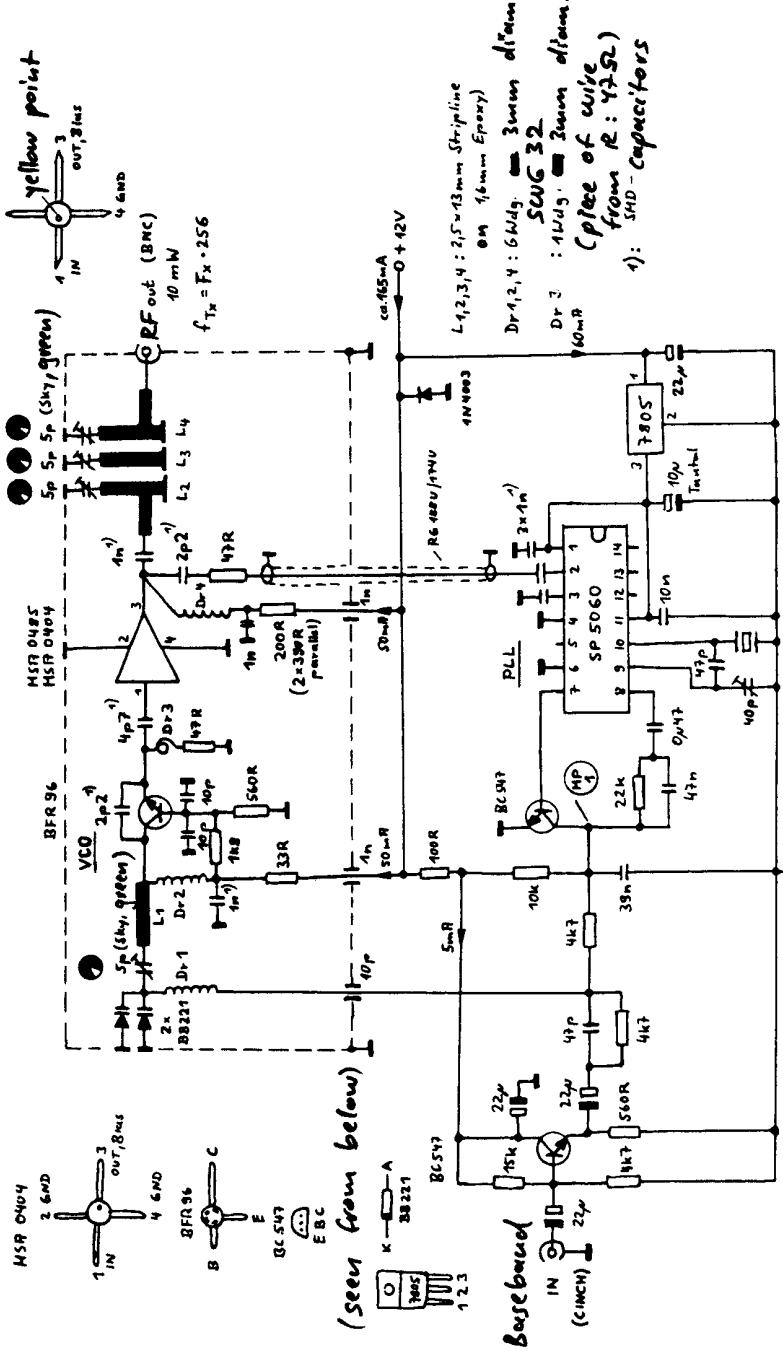


Fig.5 PLL-Locked Transmitter.

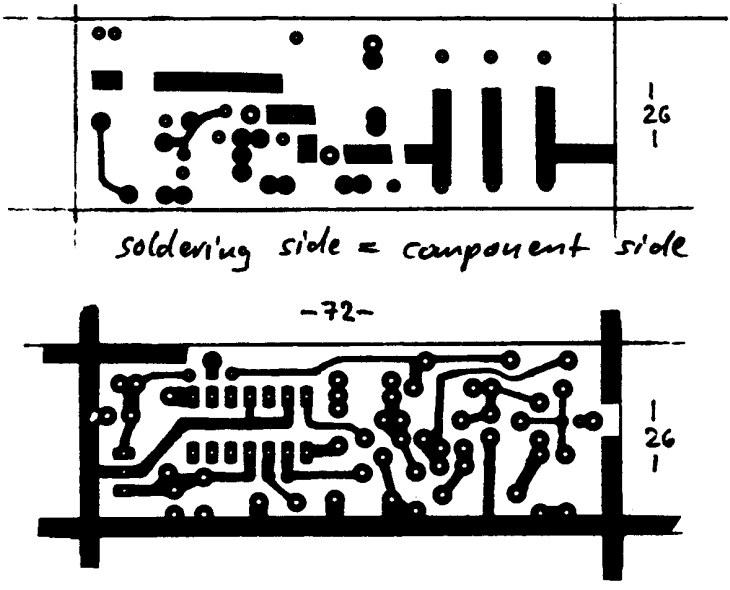


Fig.6 PCB layouts of Transmitter Boards (actual size).

ALIGNMENT

Alignment of the video and audio modulator is best conducted with the aid of an oscilloscope and a frequency counter. Connect the counter across the 100-ohm output level potentiometer. Without any audio input applied, adjust the 5uH subcarrier oscillator coil for a frequency of 5.9996MHz (U.K.) adjust appropriately if used elsewhere. Once the frequency has been set replace the counter with an oscilloscope and tune the 4uH coil for maximum subcarrier amplitude. The 9.45uH pre-emphasis coil achieves its correct value of around 10 uH by turning the core two turns inwards. Alternatively, this coil may be replaced by a fixed 10Uh choke if desired.

The only test equipment required for aligning the transmitter is a 50-ohm power meter capable of reading milliwatts. The trimmers should be preset in the positions shown on the circuit diagram (Fig.6). A regulated 12 volt DC supply is required capable of supplying around 200mA (a total of around 300mA is required for both assemblies). Connect the RF output to the power meter and ensure that the system is terminated in 50-ohms. With the trimmers adjusted as shown the voltage present on test point MP1 in the VCO section should be approximately 8.5V. If this is not the case, and after checking for errors, adjust the 5pF VCO trimmer to achieve the correct voltage. The three trimmers tuning the output stripline filter are adjusted for maximum output power as indicated on the power meter.

The setting of the VCO trimmer (8.5V on test point MP1) has considerable influence on the achievable frequency deviation. In the correct position a maximum peak deviation of 8MHz (27MHz bandwidth) can certainly be achieved, assuming an input composite colour video signal of 1V p-p.

If you now switch the supply voltage on and off the PLL should lock up readily each time (check at MP1 for 8.5 volts). The transmit frequency is adjustable over a small range (approximately -50kHz to +500kHz) by means of the 40pF trimmer at pin-9 of the PLL chip.

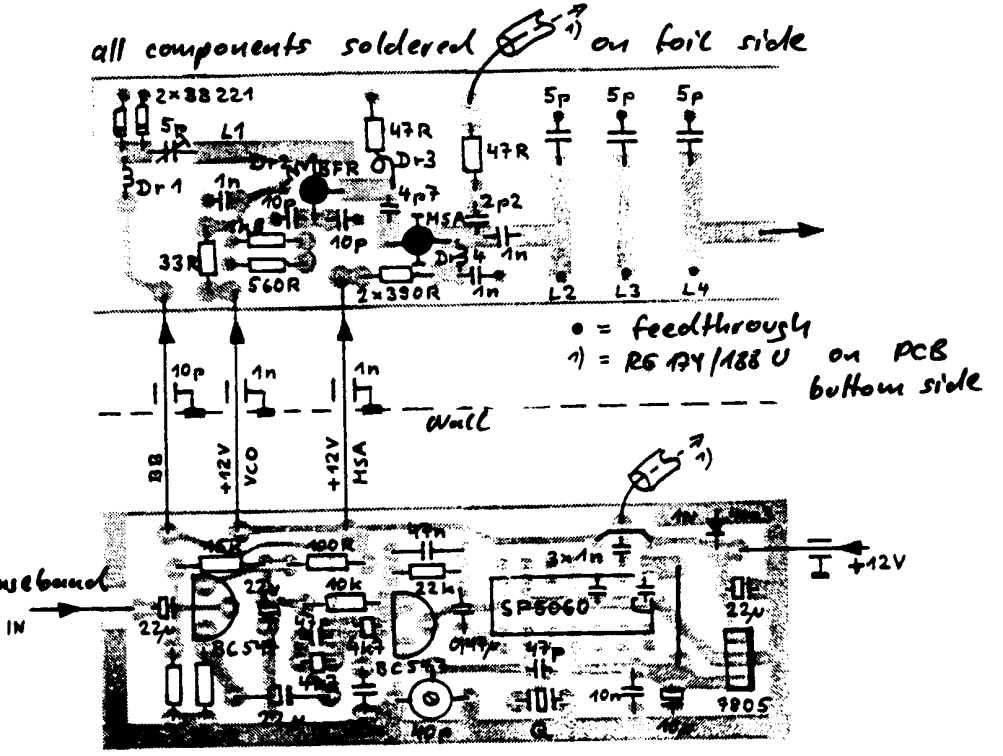
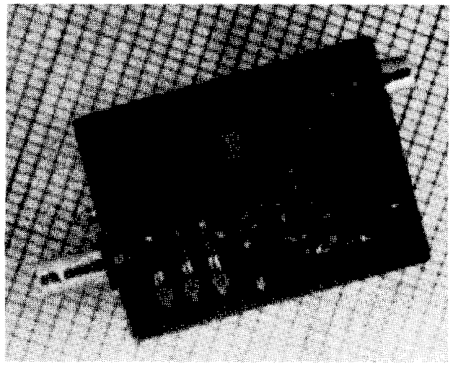


Fig.7 Transmitter circuit boards component layouts.

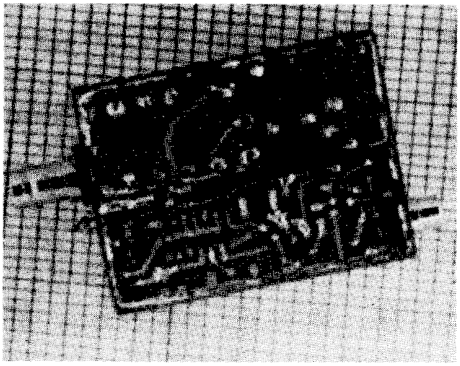
The two photographs on the following page show the transmitter assembly from above (top photograph) and below (lower photograph). After the unit has been completed and adjusted with the lids off, it should be checked that there is no frequency or power output change when the lids are in place, due to their capacity effect.

FINAL OBSERVATIONS

It is normal for the transmitter case to feel fairly warm to the touch during operation, this is not critical. If you are prepared to forego the video and audio modulator and fit an appropriate attenuator, the transmitter can be modulated directly by the video signal from a camera. This could give a pocket ATV transmitter for portable operation.



The frequency stability of the system is approximately +/- approximately +/- 500Hz, good enough even for narrowband FM use. In this case the microphone should produce a voltage of no more than 1V p-p to avoid over deviating the transmitter.



The secondary carriers (5MHz) are suppressed by around 67dB below the transmit frequency, and the second harmonic is suppressed by 53dB.

There are several ways that the low power output from this unit can be raised to a level suitable for driving larger linear amplifiers. One method would be to use a new hybrid module from Mitsubishi, the M66715. This module has around 22dB of gain and a maximum output of around 2N watts.

SPECIAL COMPONENTS

Baseband circuit: The LF356 op-amp and the BB204 Varicap diode can be obtained from Bonex, 12 Elder Way, Langley Business Park, Slough, Bucks. Tel: 0752 49502. The Neosid inductors can be obtained from Piper Communications, 4 Severn Road, Chilton, Didcot, Oxon, OX11 0PW. Tel: 0235 834328.

Transmitter circuit: The SP5060 IC, the MMIC, the varicap diodes and the Thorn 809 series trimmers are available from Bonex as above. Sky series trimmers are available from Piper Communications as above.

Suitable tin-plate boxes are available from Piper Communications under stock number 7764/25.

A 3CM ATV TRANSCEIVER

This 'second generation' transceiver has been designed to give improved performance and remove most of the problems inherent in the more common in-line conversion approach. When used in conjunction with a medium sized dish aerial (30 inches) picture strengths of P4 and better can be received over hundred kilometre plus line-of-sight paths. The transceiver uses separate transmit and receive heads for better performance and flexibility. An output power of between ten and twenty milliwatts can be expected. The receiver is of the double conversion type and tunes from 10050 to 10450 MHz. A noise figure of around 8dB is to be expected.

A set of printed circuit boards for this project is available from Members' Services, please consult the latest CQ-TV for details. This set of boards excludes the audio subcarrier generator, microphone amplifier and the sound demodulator and output, which can be easily constructed using Vero board. The printed circuit board layouts have been included for the head unit boards and the tunable IF, for those who already have working systems and wish to expand or experiment.

THE TRANSMITTER

GUNN DIODE MODULATOR

The modulator provides an adjustable modulated supply for the Gunn diode oscillator and is shown in Fig.1, with the component overlay in Fig.2. The output range is from 6 to 9 volts and can source a maximum current of 200mA. The video signal, at a level of up to 300mV p-p, is superimposed onto this supply, and is sufficient to fully modulate most types of Gunn oscillator. The Solfan head, for example, requires around 70mV per megahertz of deviation.

TR1 provides regulated 10 volts from the 12 to 15 volt main supply.

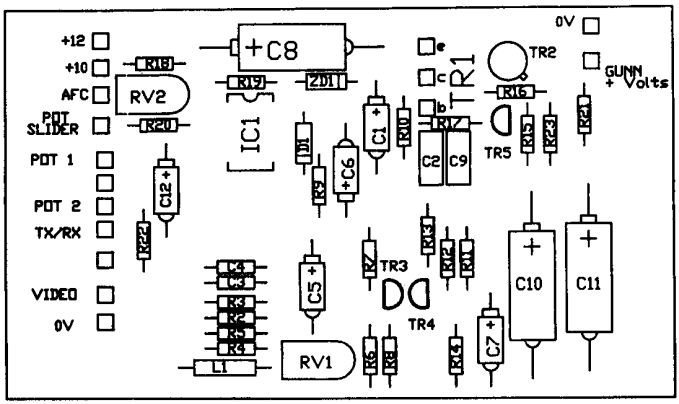


Fig.2 Modulator PCB component overlay.

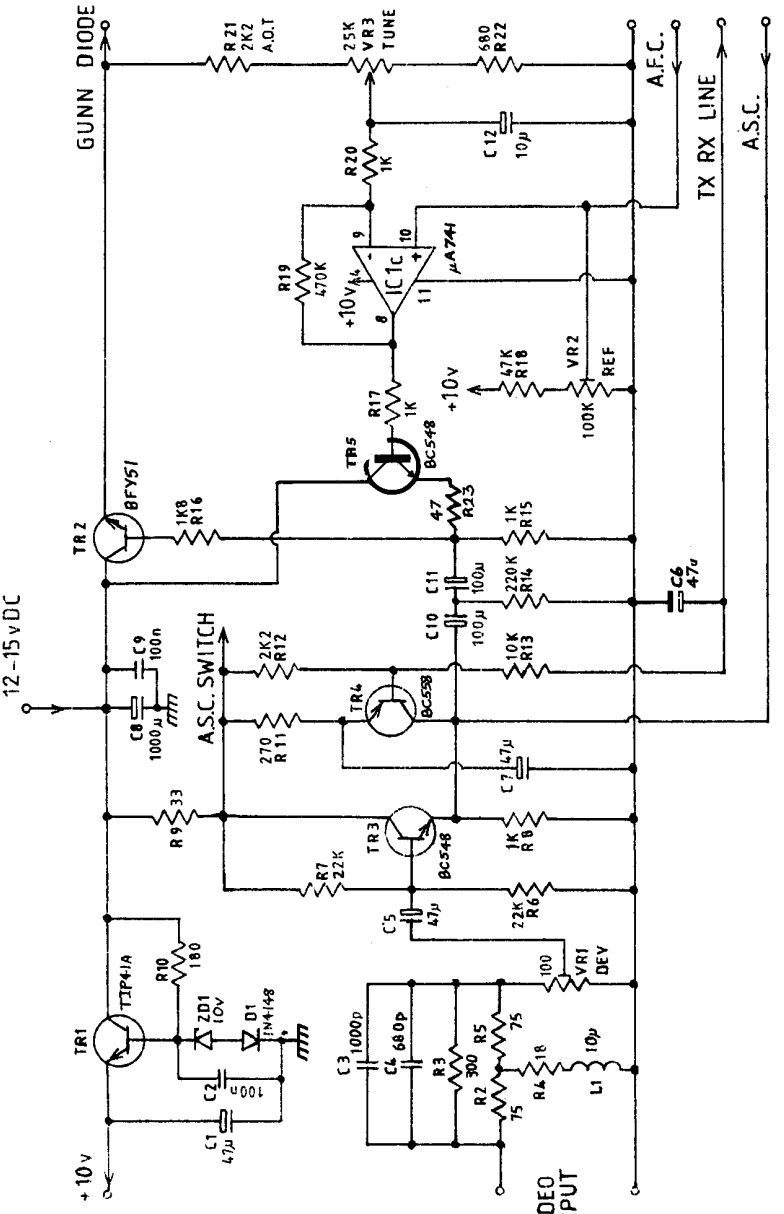


Fig.1 Gunn Diode modulator.

The Gunn diode supply regulator consists of pass transistor TR2 - which should be fitted with a heatsink - controlled by IC1c and TR5. Regulation is achieved by the reference voltage on pin-10 of the IC being compared internally to the output sample voltage on pin-9. The reference voltage is taken from the 10 volt supply via R18 and VR2. The IC is also supplied from the 10 volt rail. VR3 is the tuning control, allowing the frequency of the Gunn diode oscillator to be adjusted through a range pre-determined by the value of R21 (nominally 2k2) which should be selected on test when initially commissioning the transmitter. An automatic frequency control (AFC) input is provided and connects to pin-10 of IC1c. This is for those wishing to experiment with a phase lock loop (PLL) device such as the NE564, which could be powered from the on-board 10 volt supply.

The video input is routed via a standard CCIR pre-emphasis network (CQ-TV 131 p75) which could be made switchable with a 6dB attenuator, to enable flat band or pre-emphasised pictures to be sent (the attenuator equalises the amplitude by giving the same through loss as the network). The output of the network/attenuator is fed to TR3, the level of video deviation being adjusted by VR1. The video from TR3 is routed to the Gunn diode regulator through C10 and C11, causing the voltage to swing about the mean, and hence frequency modulating the carrier. The sound subcarrier is also fed via C10 and C11 to the regulator. Transmit/receive switching is achieved by TR4. During transmit the PTT line is held (via the PTT switch) at 12 volts, causing TR4 to turn off and Tr3 to conduct. In receive, the PTT line is held at 0 volts, turning on Tr4 and hence turning off TR3 by applying 12 volts to its emitter. The sound subcarrier input is suppressed in the subcarrier generator during receive. It is advisable to use the recommended device (BC558) for Tr4 as it exhibits a low emitter to base capacitance and thus minimises signal leakage.

Assemble the modulator using the component overlay in Fig.2. (Please note: the component overlay supplied with the PCB may be incorrect and show transistors TR3, TR4 and TR5 wrongly positioned). TR2 must be fitted with a heatsink, similarly, if the 10 volt regulated supply derived on the modulator board is to be used elsewhere in the unit, TR1 must be fitted with a heatsink.

SOUND SUBCARRIER GENERATOR

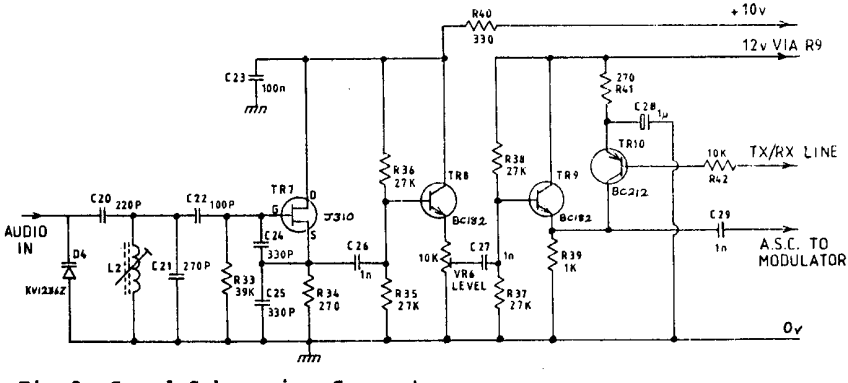


Fig.3 Sound Subcarrier Generator.

The circuit of the sound subcarrier generator is shown in Fig.3. The subcarrier is developed by a Colpitts oscillator based around TR7. The frequency of the subcarrier is adjusted by L2 and should be set to 5.9996MHz (U.K.). The audio signal is frequency modulated onto the subcarrier by varicap diode D4 which is a high capacity type, as found in the tuning circuits of modern MW radios. The specification for the diode is such that it exhibits a capacitance of 300pF at a bias of 3 volts. The specified KV1236z device is fairly expensive, so it may be worthwhile experimenting with several lower capacitance types in parallel to give the required value.

TR8 acts as a buffer for the oscillator and TR9 routes the subcarrier to the Gunn diode modulator. The level of the subcarrier is adjusted by VR6. Suppression of the output during receive is effected by switching transistor Tr10. This transistor is actuated by the PTT line and its operation is as described for TR4 in the modulator circuit.

This circuit, along with the microphone amplifier described next, are not specific to this project and may not be required by some constructors. Thus, as stated earlier, PCB's have not been made available, but due to the simplicity of the circuits they may easily be constructed using Vero board.

MICROPHONE AMPLIFIER

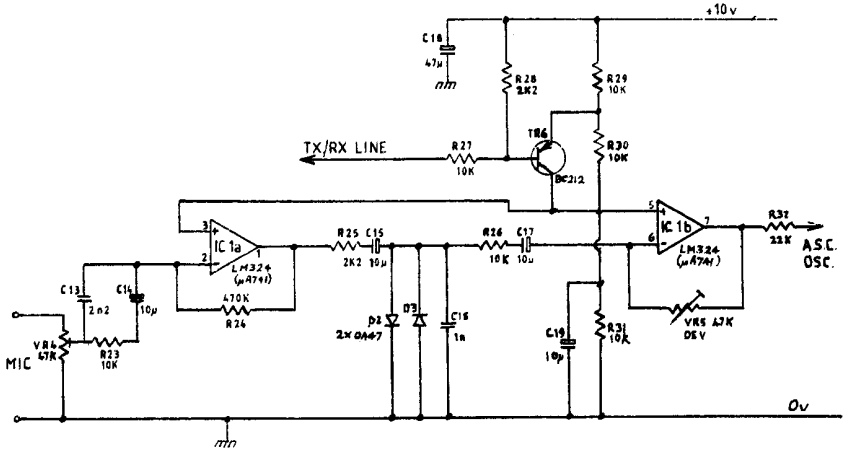


Fig.4 Microphone Amplifier.

The audio signal from a microphone requires considerable amplification before it can be modulated onto the subcarrier. A suitable circuit is shown above in Fig.4, where this amplification is carried out by IC1a and b. Diodes D2 and D3 act as a simple limiter and should be germanium types. The biasing network of R29, R30 and R31 at pin-5 sets the DC output voltage at pin-7 of IC1b to about

3.3 volts. This voltage acts as the bias supply for varicap diode D4 in the subcarrier generator, and centres the range of capacitance swing of the diode.

During receive, although the subcarrier is not routed to the modulator, it is still running. To stop any interference between the incoming sound subcarrier and this internally generated one, TR6 is included in the circuit. Turned off by the low on the PTT line during receive, TR6 switches R30 out of circuit increasing the voltage on pin-5, and hence the output DC voltage to D4 in the subcarrier generator. This in turn alters the frequency of the subcarrier such that it does not interfere with that being received. A microphone level control VR4 and an audio deviation control VR5 are also provided.

SETTING UP THE TRANSMITTER

Connect a 1k/2W resistor, or a 12V/1.2W lamp, to the output of the modulator. set the wiper of the tuning volts control VR3 to its end nearest R21. With a voltmeter connected across the output load adjust the REF voltage potentiometer VR2 to give a reading of 6 volts. Advance VR3 and monitor the output voltage which should increase to a maximum of 9.5 volts. Apply a 1 volt peak-to-peak video signal. Adjust the video deviation control VR1 (DEV) to give approximately 200mV of video modulated onto the output DC voltage.

WARNING: Gunn diodes are negative resistance devices, the lower the bias voltage, the lower the resistance and hence the higher the current. If bias below +5.5 volts is applied to the Gunn diode it may be damaged. Also, NEVER look into a head unit with the power switched on. Similarly, it is inadvisable to look into, or stand in front of, an illuminated dish or launching unit. MICROWAVE RADIATION CAN BE DANGEROUS.

Having established that all is well connect the transmit head unit and, with no video connected, set the tuning control mid-way and tune the head unit to 10.250GHz. Assuming that access to an SHF frequency counter is not possible an alternative method for tuning a head is given here (see Fig.5).

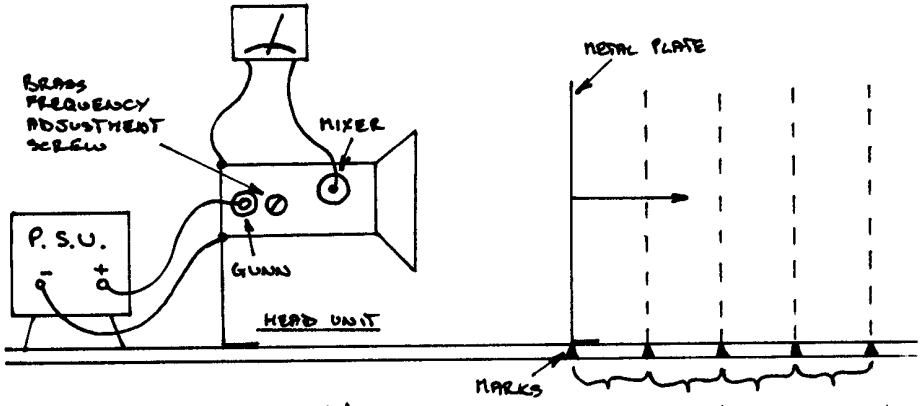


Fig.5. Head Unit tuning.

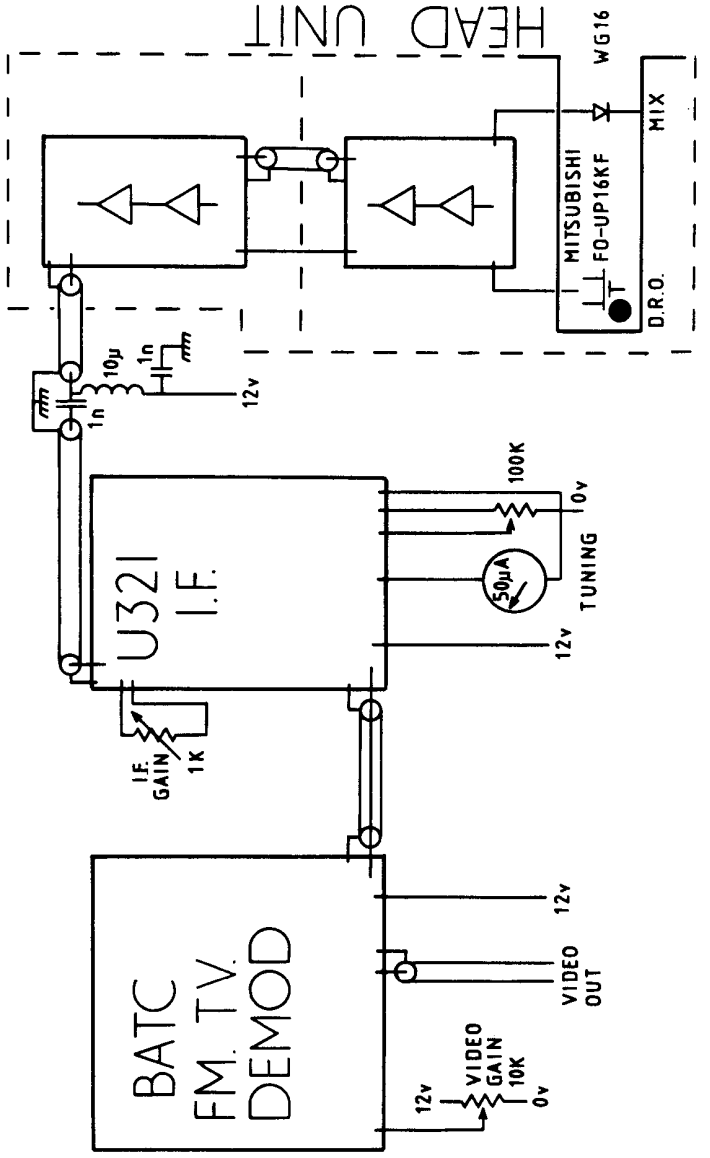


Fig.6 Receiver Block diagram.

Remove any components at the Gunn diode and mixer diode connections on the head unit. (Whilst microwave devices of this type are not particularly sensitive to handling, it is advisable to keep any contact with unconnected Gunn diodes to a minimum. Also, the use of isolated soldering equipment is recommended).

If a Solfan head is being used then it is likely that the oscillator will be set to around 11Ghz. Initially undo the brass locknut and screw in the brass screw by 1-turn. DO NOT move the steel screws yet. Fix the head unit firmly to a flat surface and apply about +7.5 volts to the Gunn diode. Connect a multimeter between the mixer diode and ground (Fig.5) with the Gunn supply on a current of between 1 and 3mA should be shown on the meter. Take a flat piece of metal and, keeping it parallel to the mouth of the horn, move it slowly away and watch for a minimum reading on the meter. When this condition occurs mark the position of the plate. Continue moving the plate outwards until another position of minimum current is found and again mark the position of the plate. The distance between the two marks is half the wavelength of the oscillator and from this can be determined the frequency.

The accuracy of this method can be improved by finding several minimum positions and averaging the result. If the frequency is not correct make small adjustments to the BRASS screw until the correct frequency is obtained, turning the screw in reduces the frequency and screwing it out raises it. The following equation is used to determine the actual frequency from the wavelength measurements:

$$\text{Frequency} = \frac{150}{\text{distance in millimetres}}$$

If a transmit head unit other than the Solfan type is used, the same method as above can be employed to calculate and thus set the oscillator frequency, but some experimentation with the tuning screws will be required to ascertain the correct procedure.

That completes the setting-up procedure for the transmitter, and you should now be developing in the region of 10mW of 3cm FM television.

These three modules make up the transmit part of the system, and once again show how relatively simple equipment can be at these frequencies. The receiver in this system is where the changes have been made, and although it is rather more complex than our previously published systems, by using 'state-of-the-art' technology a very sensitive, but easily constructed design has been achieved.

THE RECEIVER

THE HEAD UNIT

A block diagram of the receiver chain is shown in Fig.6. This shows that a totally new approach has been taken. Instead of the usual Solfan type receive head employing a conventional Gunn effect mixer diode, a heterodyne GaAsFET Microwave receiver (block converter) is used. This block converter is a Mitsubishi FO-UP16KF module (Fig.7) which contains a stable GaAsFET Dielectric Resonance Oscillator (DRO) and a Schottky diode mixer, housed in a section of waveguide fitted

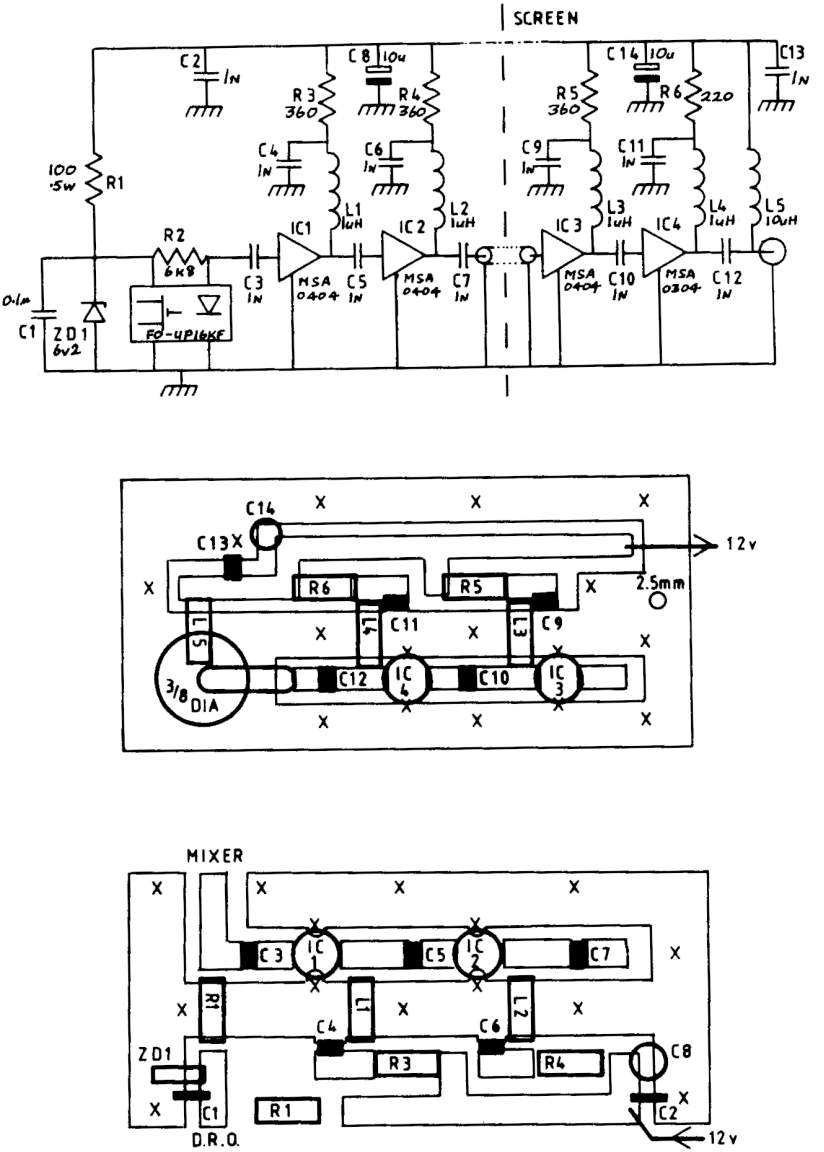


Fig.8 Mitsubishi Head Unit and MMIC amplifiers.

with a waveguide sixteen flange. The DRO requires a stable 6 volt supply and for our purposes must be tuned to 9.60GHz.

There is a small amount of leakage from the 9.6GHz local oscillator within the module. In some cases it may be advisable to fit an isolator or filter between the converter and the aerial. A design for a suitable filter may be found in the RSGB VHF/UHF manual, fourth edition, on page 9.38.

Mounted onto the block converter is a two-stage first IF amplifier, the circuit and circuit board component overlays of which are shown in Fig.8. Printed circuit board layouts are shown actual size in Fig.9. The amplifier is constructed using Monolithic Microwave Integrated Circuits (MMIC,s) which return very high gain for simplicity in design. The MMIC amplifier is divided into two stages which should be screened from each other to maintain stability. The IF frequency from the mixer will be in the range 450 to 850MHz over the range 10.05 to 10.45GHz, and the MMIC amplifier will produce well in excess of 50dB of gain.

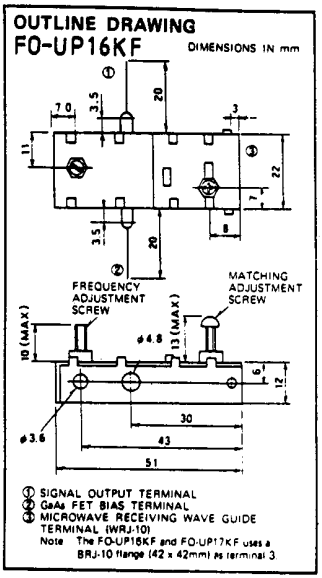
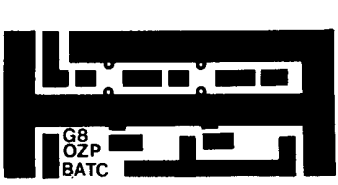
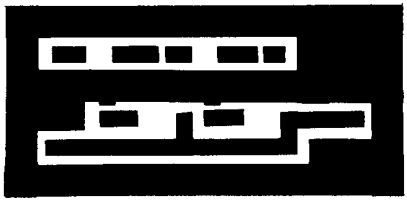


Fig. 7 Head module.

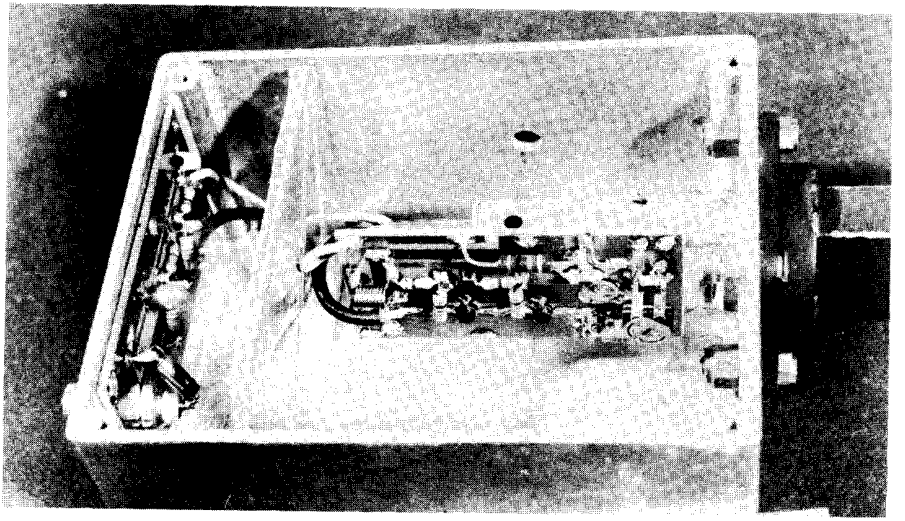
The head unit is powered by 12 volts DC fed up the coaxial cable connecting it to the second IF unit as shown in the block diagram. The stabilised supply for the converter is provided by R1 and ZD1. The whole assembly must be mounted into a good quality RF proof enclosure, with a screen between the two twin MMIC stages. The MMIC devices are relatively robust and no particular handling techniques need be employed. The converter however is static-sensitive and care should be taken whilst handling and soldering. Once it is connected into the unit it can be subjected to normal handling. Good high-frequency RF construction techniques are essential in the building of this assembly. A photograph of a completed unit is shown in Photograph-1.





Board-1 Board-2

Fig.9 Head unit printed circuit board layouts, actual size.



Photograph-1. The Mitsubishi module Head Unit

As an alternative approach to the above a Solfan receive head could be used, or even a Ku-band satellite TV converter. A description outlining the use of either is given below.

SOLFAN BLOCK CONVERTER

The widely available Solfan mixer module is not suitable as it stands for an ATV receive converter. This is due to the relatively high value of decoupling capacitance built into the diode mount. However, the oscillator may be retained as the local oscillator and a new mixer constructed using a 1N23 diode (Photograph-2).

The oscillator will not tune down to 9.6GHz to give the required 450n to 850MHz IF range. Instead, the oscillator should be set to 10.9GHz, this will give reversed tuning and inverted video. The former will not cause any problems other than the tuning dial working in the opposite direction, the latter can be rectified at the video demodulator, which is switchable between video senses.

The mixer should be constructed out of a piece of waveguide-16 as shown in Fig.10, the dimensions are given in millimeters unless otherwise specified. The length of the section of waveguide is not critical, but should be long enough to house the first stage MMIC head amplifier. R1, C1 and ZD1 on the MMIC board (Fig.8) are not required in this instance. Fig.11 shows the mixer diode supply regulator circuit, which can be built self-supporting onto the diode connections. A heatsink for the regulator is not required.

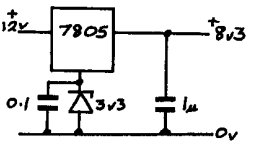


Fig.11 Mixer supply

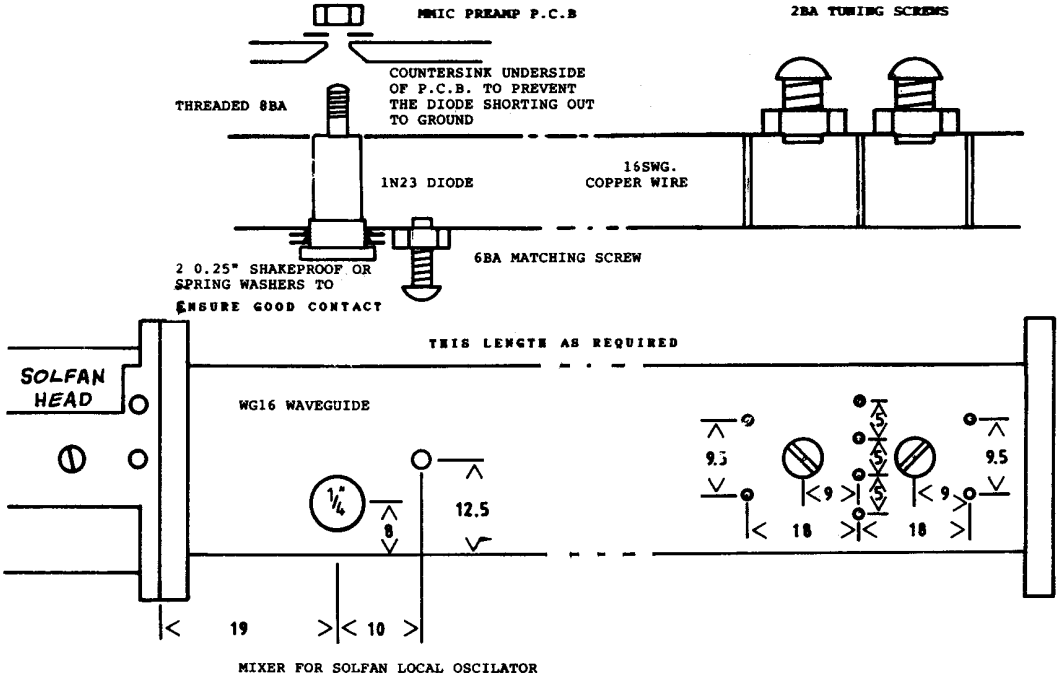
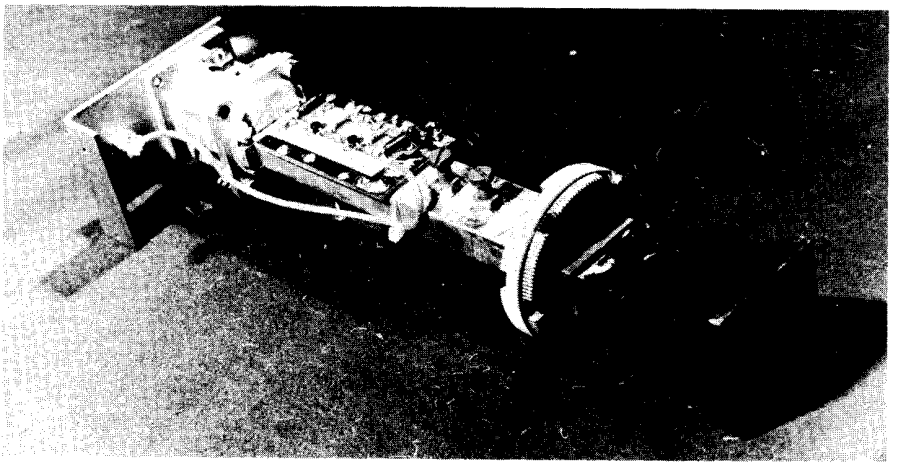


Fig.10 Mixer for Solfan receive head.

A hole should be drilled in the input line of the MMIC amplifier board to enable it to be mounted direct onto the mixer diode as shown in Fig.10. A 10uH choke should be connected from the same point to ground to act as a DC return path for the diode. The second stage MMIC board should be mounted in a separate screened enclosure and connected to the mixer assembly using miniature screened coax.

The filter section is based on the design in the RSGB VHF/UHF handbook fourth edition (page 9.38) and is required to prevent radiation of the 10.9GHz local oscillator. Initially mark a centre line onto the length of waveguide. Next mark the position of the tuning screws and the 16SWG wires (these wires can be constructed from the conductors of 2.5mm twin and earth mains cable). Drill all the holes and carefully remove any burrs from inside the cavity. Feed the wires though the holes, ensuring that they remain straight, and crimp them in place. If they are to be soldered in position this must be carried out from underneath, so as to avoid any excess solder from entering the cavity. (Solder is a very lossy substance at microwave frequencies). The locking nuts for the tuning screws can be similarly soldered to the waveguide, or alternatively fixed in place using epoxy resin. To simplify construction a waveguide isolator can be used instead of the filter, however these are somewhat difficult to obtain. The completed unit should be fitted into a screened box in order to prevent problems with broadcast interference. The set-up procedure for the local oscillator is the same as described for the Mitsubishi module in the 'Setting Up The Receiver' section below.

The use of Gunn diode for the local oscillator and a separate mixer diode will unfortunately give a higher noise figure than that exhibited by the previous system. It has been noted that the local oscillator 'pulls in frequency as the loading changes, thus it will be necessary to confirm the frequency of the oscillator whilst tuning. Also high receive signal levels can cause the same problem.



Photograph-2. A modified Solfan receive head.

SATELLITE LNB CONVERTER

Some satellite TV LNB's (Low Noise Blocks) can be converted for use on the 3cm band, how this is achieved will depend upon the make being used. The author uses a converted SAT-TEL model FB3 LNB, the performance of which is very good.

The local oscillator in LNB's is of the Dielectric Resonance Oscillator (DRO) type and for the more common 10.9 to 11.7GHz types runs at 10GHz. A tuning screw is generally fitted giving a range of around +/-100Mhz. The factors affecting the resonant frequency of oscillation are the position of the DRO in the cavity, its thickness and composition.

The method for converting the FB3 LNB is quite simple and is as follows: Remove the three screws from the end of the case and pull off the cover, this may be a very tight fit. Remove the ten screws to gain access to the RF amplifier, mixer and DRO. The DRO is held in place with a glue which can easily be broken, thus freeing the DRO chip.

Reducing the thickness of the DRO chip increases its resonant frequency, but by how much and the exact position to refit it has to be found by trial and error. It is best accomplished with a personal beacon running at 10.250GHz, or by using a known frequency source and a receiver such as an R7000. Grind down the chip using grade-300 Emery paper on a flat surface and replace it over the gate and source lines from where it was removed and check the frequency. Repeat this procedure as necessary until the oscillator is running at approximately 10.9GHz. The final frequency can then be adjusted using the tuning screw. As the frequency increases the positioning of the DRO chip becomes more critical for reliable oscillation. When the oscillator is running about S9 of noise should be indicated, or solid white noise on the monitor of a 10GHz receiver. Once the DRO has been 'adjusted' refit it in position using a tiny spot of clear nail varnish. The tuning screw will now give approximately +/-50Mhz shift in frequency.

The IF amplifier fitted to the converter is wide band and generally has sufficient gain at 10.250GHz. This amplifier is located behind the mixer/oscillator board, and its performance may be improved by adjusting the two small trimmers located on the board. Further IF amplification may improve results and it is recommended that the second-stage MMIC IF amplifier is used. The FB3 LNB will work satisfactorily at 12 volts and the necessary components for feeding the supply via the coax cable is shown in Fig.12 and in Photograph-3.

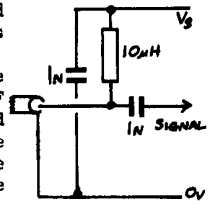
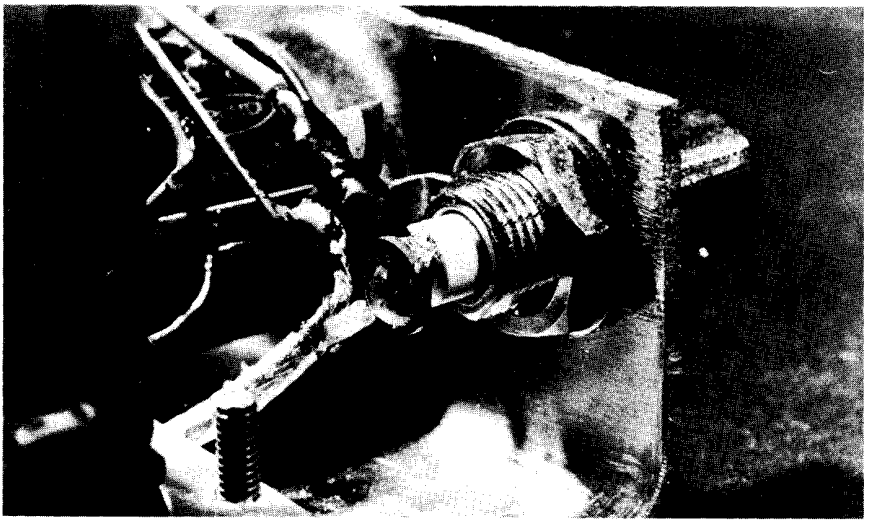


Fig.12

The waveguide used on LNB converters is generally WG-17, To allow this to be used with WG-16 a transition should be constructed using a 6cm length of waveguide-16 with a size 16 flange at one end and a size 17 at the other.

As the oscillator is running on the 'high' side again at 10.9GHz, the necessary changes noted in the section above describing use of a Solfan receive head will be found.

A modified FB3 LNB converter is shown in Photograph-4.



Photograph-3. Feeding the DC supply for the LNB via the coax.

TUNABLE IF STAGE

The tunable IF is built around a domestic Philips U321 television tuner. The output from the head unit is fed into the aerial input of the U321. Within the tuner, the IF signal is first amplified, then fed through a bandpass filter to the mixer stage. The internal voltage controlled local oscillator mixed with the amplified head unit IF produces a second IF around 35MHz, which is further amplified and output to the demodulator stage.

The final stage of the U321 tuner is another bandpass filter. However, owing to the wide bandwidth of a frequency modulated television signal this filter must be disabled. This is effected by shorting-out one of the filter inductors as shown in Fig.13.

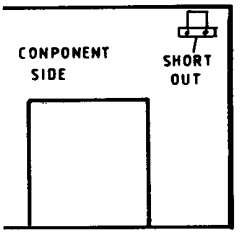


Fig.13 U321 O/P mod.

The external control circuitry for this stage is shown in Fig.14, with the component overlay and PCB layout in Fig.15. The voltage controlled oscillator in the tuner requires a variable 0 to 30 volt supply for the tuning diode. This is generated by an NE555 (IC1) oscillator driving a voltage multiplier, comprising D1 to D6 and C8 to C13. The output from the voltage multiplier is stabilised by R5 and IC2, which should be a TAA550 or similar 30 volt regulator as used in television receivers. The tuning control, which may be mounted remotely from the unit if desired, should be a 100k ten-turn wirewound potentiometer fitted with a multi-turn dial. A tuning meter may be fitted as shown in the diagram, this should have a 50uA FSD movement, R7 being the necessary shunt

resistor. A meter having a higher FSD movement cannot be used as damage may be caused to the current source inside the U321 tuner.

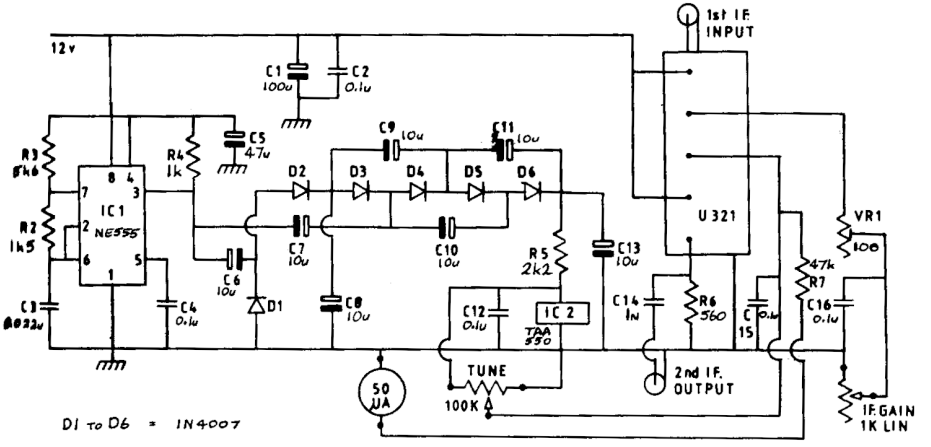


Fig.14 Tunable IF control circuitry.

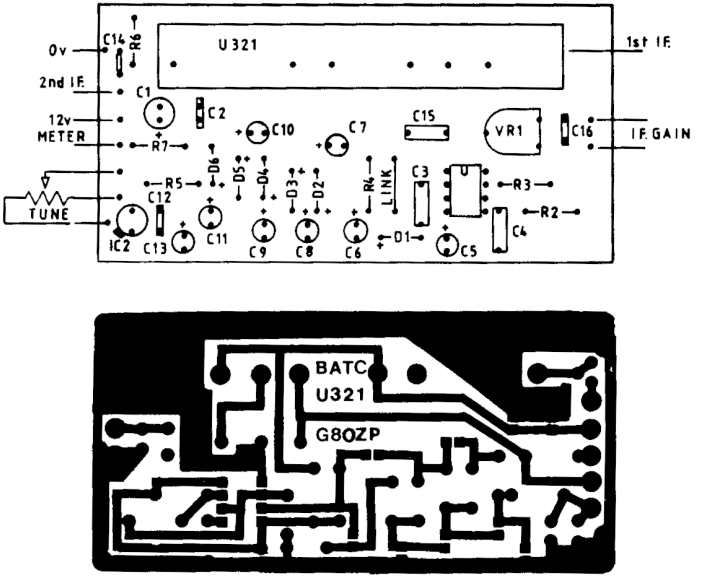
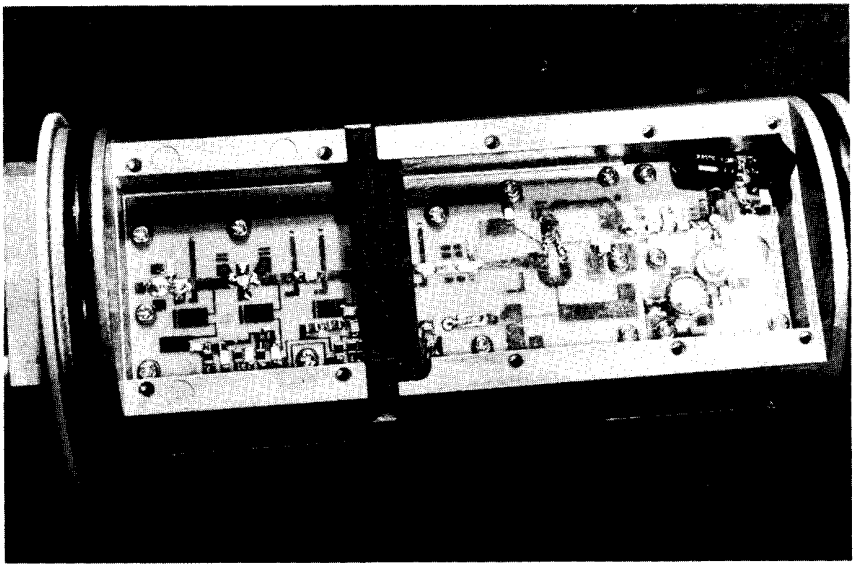


Fig.15 Tunable IF component overlay and PCB layout.



Photograph-4. A modified Ku-band FB3 LNB converter.

VIDEO DEMODULATOR

The video demodulator used in the prototype is a modified version of the BATC 'FM-TV Demodulator' (CQTV122). The now modified circuit is shown in Fig.16. (The original printed circuit board and component overlays supplied with the kit of boards are still used for this modified circuit, please refer to the instructions detailed in the section on construction). The output from the tunable IF is fed into TR1, a dual-gate MOSfet giving high amplification with low noise performance. The signal passes to an NE592 (IC1) wideband amplifier , with VR1 operating as the stage gain control. The output of IC1 passes directly to the NE564 (IC2) which in this modified design is configured as a phase comparator. In this mode the NE564 operates using a free-running VCO set to the average IF frequency, rather than the original design whereby the VCO tracked the incoming signal. This change obviates any need to occasionally re-tune the VCO, also it appears rather less 'touchy' to set up.

The demodulated video signal passes through an emitter follower (TR2) where the sound subcarrier is extracted and routed to the audio subcarrier demodulator board via R19 and C19. The video then passes through a CCIR standard de-emphasis network, which could be routed through a switching network if required to allow for reception of non-emphasised video signals. If this system is adopted leave R21, R22, R23, R24, R25, C20, C21 and L2 off the board. Connect the emitter of TR2 direct to C22/L3. The de-emphasis network is built separately and switched into the video output lead. A 6dB attenuator network must be switched in place of the de-emphasis network in order to maintain a constant video level).

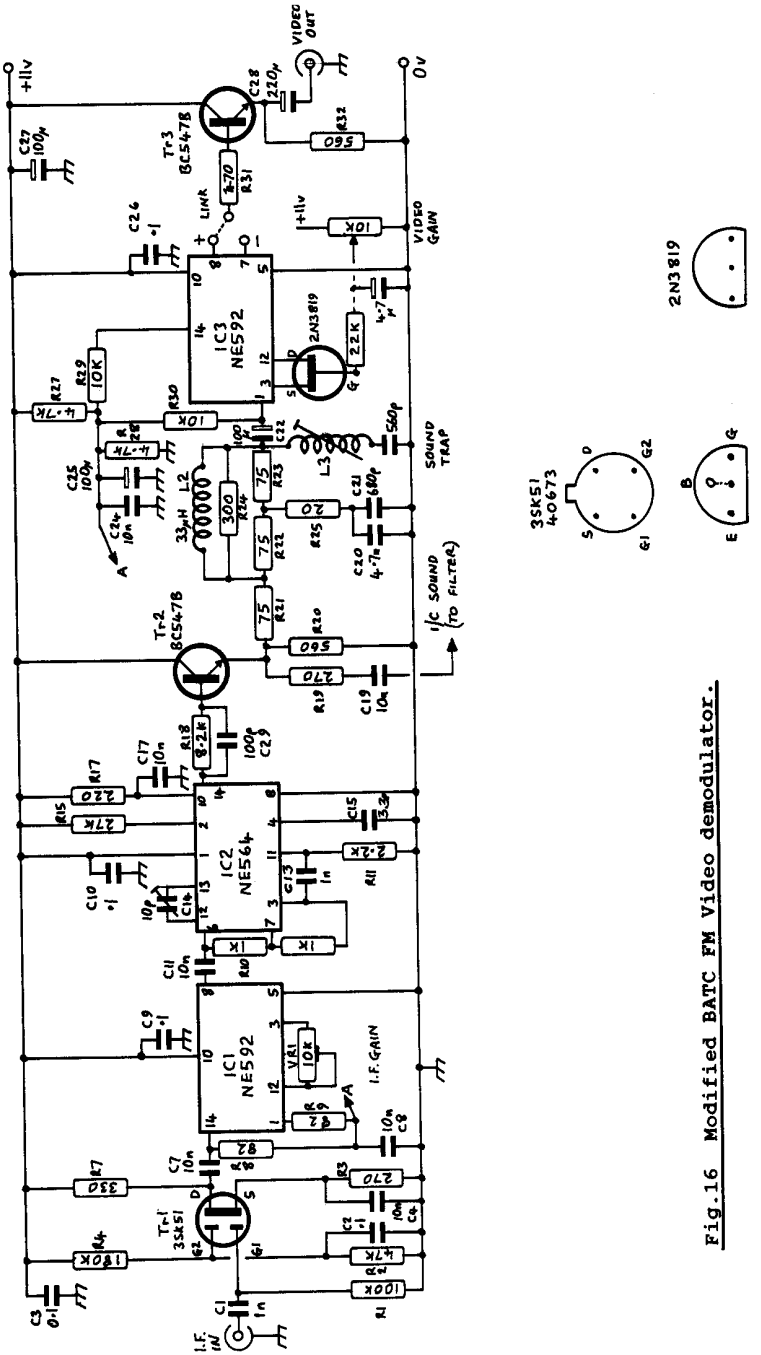


Fig.16 Modified BATC FM Video demodulator.

The output from the de-emphasis network is fed to IC3 - a second NE592 - this time acting as a video amplifier. This stage is where the second major modification to the original design takes place. In the original design the video gain control was an on-board potentiometer, however for this design it is advantageous to have this control mounted remotely from the board on the control panel. In order to achieve this an FET transistor is used. As the remote gain control is varied the transistor is gradually switched on or off, dependant on the direction of rotation. This change in the state of the transistor causes the source to drain resistance to vary, which in turn varies the resistance between pins-3 and 12 of the IC, thus controlling the stage gain.

There are two outputs from IC3 providing both positive and negative going video signals. Provision is made to switch between these outputs enabling both standards to be received. TR3 is another emitter follower providing a 75-ohm video output for feeding direct to a monitor.

AUDIO DEMODULATOR AND OUTPUT STAGE

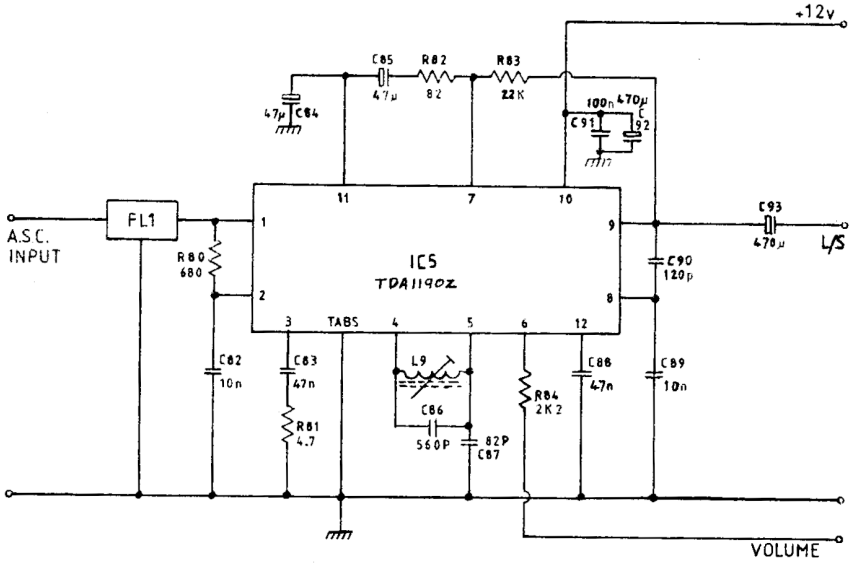


Fig.17 Audio Demodulator and Output.

A single chip design is used for the audio demodulator and output (Fig.17) built around the TDA1190Z (IC5). The incoming audio subcarrier is fed through a 6MHz ceramic filter (FL1) to the limiting amplifier within the IC. L9 is tuned to 6MHz and acts as the load for the internal quadrature detector. The volume control is a 22k potentiometer connected between pin-6 and Ø volts, R84 is included to maintain stability and stop self-oscillation. Reducing the resistance

of the volume control increases the audio output from pin-9, which at a maximum will be about 1.5 Watts into an 8-ohm load. Although the device has cooling fins, it is advisable to provide extra heatsinking if it is to be used at high output for prolonged periods.

N.B: A TDA1190 may be used instead, in which case the volume control should be 2.2k in value, and R88 and R84 removed from the circuit.

CONSTRUCTION

The block converter is best housed in a diecast box measuring approximately 5" x 4" x 2.5". The cut-out to match the waveguide 16 input should be accurately filed and two small holes drilled in the box to provide access to the tuning screws for the DRO and input matching. Assemble the two head unit circuit boards ensuring that all component leads are as short as possible and that the minimum of solder is used, also ensure where applicable that components are soldered to BOTH sides of the PCB (ie: use good UHF/SHF construction techniques). The soldering on the ground plane side of the boards should be maintained as low-profile as possible to enable the boards to be fitted correctly.

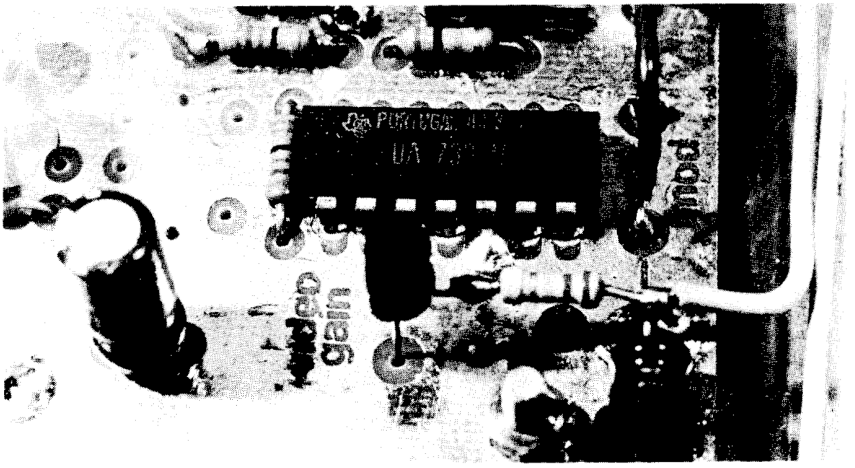
The first-stage head board is soldered to the converter module at three locations; either side near to the flange and once at the rear. These locations are chosen such that the fixing tags on the converter can be bent over and soldered to the PCB without shorting other connections. Use a hot soldering iron and make the joints quickly, it may be useful to have a can of 'freezer' handy to cool down the body of the converter after each connection is soldered.

The connection between the first and second-stage head boards should be made with miniature co-axial cable. The output connection from the second-stage board to the BNC socket should be made using a short length of 2.5mm brass or copper strip. The 12 volt supply feed inductor L5 should be connected direct to the output BNC socket using a minimum lead length. Connection between the complete head assembly and the IF/Demodulator assembly should be made using good quality 50-ohm coaxial cable. The 12 volt supply for the head unit is fed in as shown in the block diagram (Fig.6).

The tunable IF and demodulator boards should also be fitted into an RF proof diecast enclosure to minimise broadcast channel interference (BCI) as they are operating within the terrestial TV UHF band. The 12 volt supply should be fed into the assembly via a 1nF feed-through capacitor and a 10uH choke (ensure that the choke is capable of handling the current drawn). If a remote IF gain control is not required omit the 1k control shown on the circuit as 'IF gain' and replace C16 with a link, VR1 remains as the on-board IF gain control. IC2 may be replaced with a standard 30 volt zener diode, however, stability may be lost as a consequence, causing difficulty in tuning-in weak signals. The connection between the IF and demodulator boards should be made using miniature 50-ohm coaxial cable.

The demodulator may be built onto the original BATC board (as detailed in CQTV 122 and the 'Best of CQTV') but with some modifications to accommodate the changes to the original design. L1, R5, R6, C5 and C6 are no longer required and should be omitted, fitting a wire link in place of L1 connecting the output from the drain of TR1 to R6. The changes affecting IC3 are a little more complex as far as the PCB

layout and component overlay is concerned. Disconnect pin-9 from pin-3 by cutting the track, leaving pin-9 disconnected. C12 and C16 are not fitted, C13 is now fitted on the underside of the PCB between pins-3 and 11. R13 is now also fitted on the underside of the board between pins-3 and 7. Capacitor C29 has been added, and should be wired across R18 underneath the board. It has also been found in that the demodulator runs better with a supply of 11 volts, which can be achieved by feeding the board via a 7905 regulator IC with a 5.6 volt zener diode in series with its reference leg (the centre pin normally connected to ground). Please note that C15's earth lead is soldered direct to the ground plane on the top-side of the board. The component side track connecting R9 and C24 should be soldered on both sides at each end. The remote video gain transistor TR4 should be mounted in place of the video gain potentiometer, as shown in Photograph-5.



Photograph-5. The remote Video Gain Control modification.

SETTING UP THE RECEIVER

The demodulator should be adjusted first. Connect the 12 volts supply and check that the voltage on pin-1 of IC1 is at approximately half supply. Connect a frequency counter to IC2 pin-11 and adjust C14 to set the frequency to 36MHz (C14 is usually around half mesh). Turn VR1 to maximum (fully clockwise).

Connect the demodulator and the tuner together, along with the external IF gain, video gain and tuning controls. Apply the 12 volts supply and connect a video monitor to the demodulator output. Set the video gain control to mid-way, also the remote IF gain control and its associated on-board pre-set VR1. Disconnect the cable from the converter and also, to prevent accidents, disconnect the 12 volt feed onto the cable.

A temporary calibration dial scale for the IF tuning control should now be made: Using an audio modulated RF signal generator connected to the 'aerial' input of the U321 tuner, mark the chart at 20MHz intervals, starting at around 450MHz. When the tuning matches the input IF frequency from the generator alternate black and white bands will appear on the monitor screen. Beware of tuning into images, these can be confirmed by reducing the output of the generator and retuning, if no other signals are found then mark the scale accordingly, if other tuning ppoints are found reduce the output again and retune. This process is repeated until only one tuning point is confirmed for each 20MHz step. It should be noted here that the tuning scale will be somewhat non-linear.

Once the tuning scale has been mapped out reconnect the converter cable and the 12 volt supply feed to the head unit. A known frequency is also required to accurately set the block converter so, assuming that an SHF generator is not available, the best place to find such a known frequency is from one of the 10GHz beacons found around the country. An example of such a beacon is GB3LEX at Leicester radiating on 10.4GHz. The oscillator in the block converter is required to be set at 9.6GHz, that is 800MHz below the signal frequency. Thus, if a signal from GB3LEX is being used to set-up the converter tune the IF to the previously calibrated point for 800MHz, slacken the locknut on the adjustment screw for the DRO and carefully tune for the beacon signal (Turning the screw in increases the DRO frequency). Finally, the converter module mixer matching screw should be adjusted for maximum signal.

Having one point on our tuning scale we can confirm a second by using the previously set-up transmit module to provide a signal at 10.25GHz. This signal should tune in around the 650MHz mark on the tuning scale (ie: 10.25 - 9.6). With these two points confirmed the temporary tuning dial can now be scaled in GHz to represent the received signal rather than the IF signal.

Finally, switch on the transmitter with the tuning control (VR3) set to give 7.5 volts on the Gunn diode (ie: to give a transmit frequency of 10.25GHz). Apply a video signal and monitor the picture on the receiver. Carefully adjust the Gunn tuning volts (VR3) until maximum signal strength is obtained. Reduce the tuning volts by 0.5V and set the video deviation (VR1) for the desired picture.

GENERAL NOTES

The Mitsubishi FO-UP16KF module used in the first head unit receiver option may be difficult to locate. It may be replaced by the Mitsubishi FO-UP11K module, however some changes will need to be made. The FO-UP11K comes in waveguide-17, this size may be utilised in the whole system without any detriment. Alternatively a tapered transition maybe constructed to convert from WG17 to 16. Also, the module is not fitted with an input flange. If a flange is required one should be fitted using an adhesive, as prolonged soldering may damage the unit. The converter will not tune down to 9.6GHZ thus, as with the Solfan converter and the TVRO FB3 LNB, the oscillator should be set at 10.9GHz.

The IF frequency range is the same as used by broadcast television in bands four and five. However, breakthrough need not cause any problems if correct attention is paid to screening and decoupling.

The 50-ohm coaxial cable used to connect the head assembly to the IF board need not be of the low-loss type, but must have a good quality outer screen.

The IF gain pre-set on the demodulator board should be reset to a minimum setting consistent with good performance.

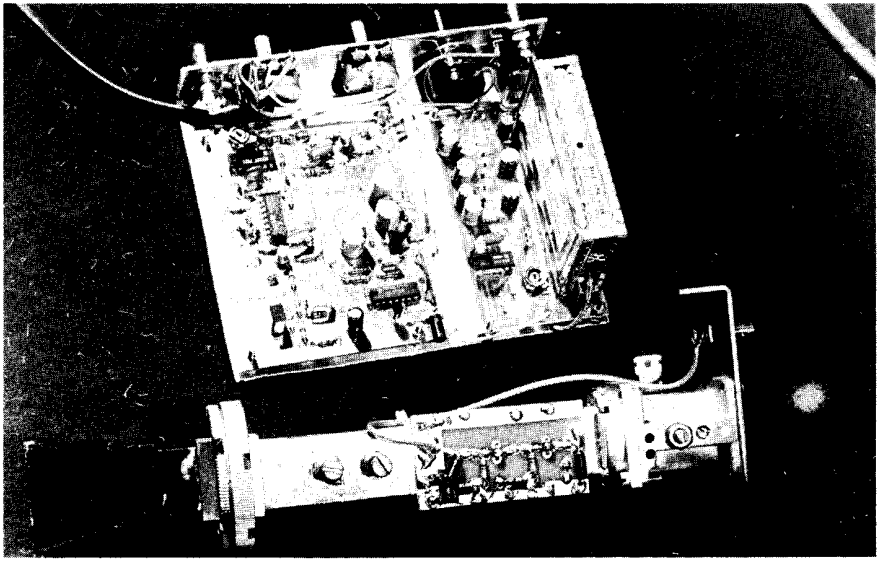
The amount of video deviation required will depend upon the Gunn head type. Excessive deviation will produce heavy contrast, flecking and sync pulling.

The tunable IF and demodulator assembly can also be used for other bands. For example: mix 23cm signals with a local oscillator set at 600MHz; mix 13cm with 1800MHz, thus resulting in an IF of around 650MHz.

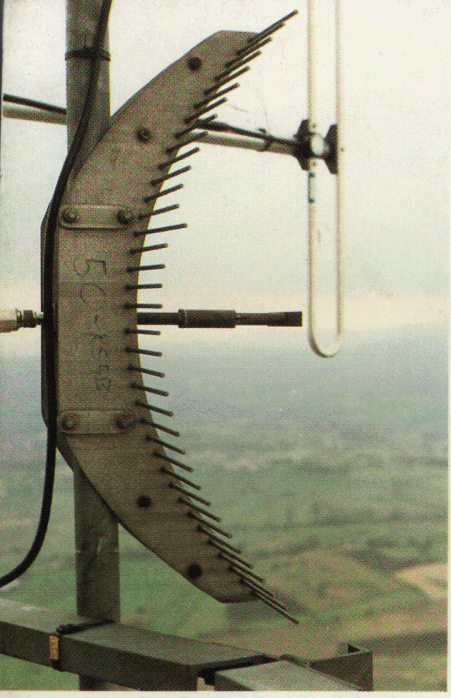
Versions of the U321 tuner are available for use with synthesisers. A study of the relevant manufacturers diagrams will reveal how this could be effected, thus giving digital frequency selection.

Finally, the converter or IF board output could be fed into a scanner covering the appropriate frequencies thus acting as a phone receiver. Similarly, if 'straight' audio is fed into the audio subcarrier input of the Gunn diode modulator board, with no video input, then you have a very good wide-band phone transmitter.

The Photograph below shows the author's completed prototype with the modules fitted to a mounting plate.

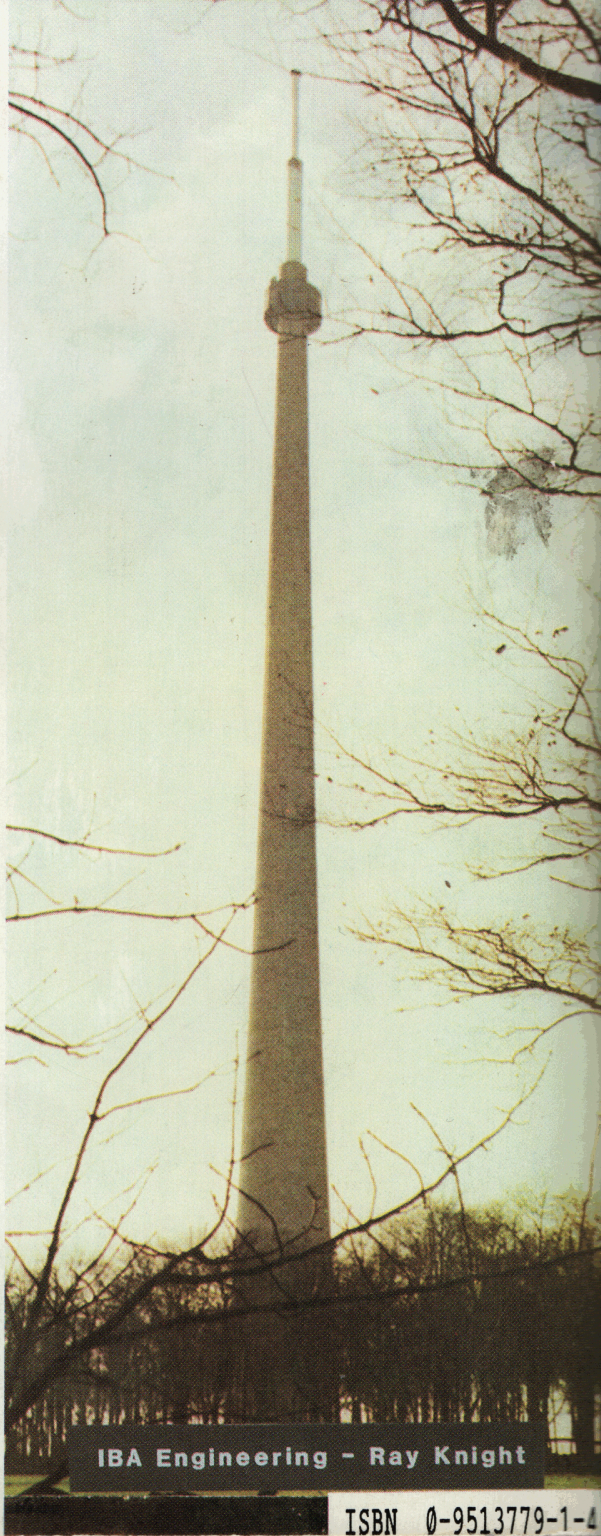


Photograph-6. The completed prototype.



GB3ET

IBA TOWER - EMLEY MOOR



IBA Engineering - Ray Knight

ISBN Ø-9513779-1-